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(To be filled in the OMR Sheet)

प्रश्नपुस्तिका क्रमांक
Question Booklet No.

O.M.R. Serial No. | | | | | | | | |

प्रश्नपुस्तिका सीरीज
Question Booklet Series
C

B.C.A.(Third Semester) Examination, February/March-2022

BCA-303(N)

Computer Architecture & Assembly Language

Time : 1:30 Hours **Maximum Marks-100**

जब तक कहा न जाय, इस प्रश्नपुस्तिका को न खोलें

निर्देश : –

1. परीक्षार्थी अपने अनुक्रमांक, विषय एवं प्रश्नपुस्तिका की सीरीज का विवरण यथास्थान सही– सही भरें, अन्यथा मूल्यांकन में किसी भी प्रकार की विसंगति की दशा में उसकी जिम्मेदारी स्वयं परीक्षार्थी की होगी।
2. **इस प्रश्नपुस्तिका में 100 प्रश्न हैं, जिनमे से केवल 75 प्रश्नों के उत्तर परीक्षार्थियों द्वारा दिये जाने है। प्रत्येक प्रश्न के चार वैकल्पिक उत्तर प्रश्न के नीचे दिये गये हैं। इन चारों में से केवल एक ही उत्तर सही है। जिस उत्तर को आप सही या सबसे उचित समझते हैं, अपने उत्तर पत्रक (O.M.R. ANSWER SHEET)में उसके अक्षर वाले वृत्त को काले या नीले बाल प्वांइट पेन से पूरा भर दें। यदि किसी परीक्षार्थी द्वारा निर्धारित प्रश्नों से अधिक प्रश्नों के उत्तर दिये जाते हैं तो उसके द्वारा हल किये गये प्रथमतः यथा निर्दिष्ट प्रश्नोत्तरों का ही मूल्यांकन किया जायेगा।**
3. प्रत्येक प्रश्न के अंक समान हैं। आप के जितने उत्तर सही होंगे, उन्हीं के अनुसार अंक प्रदान किये जायेंगे।
4. सभी उत्तर केवल ओ०एम०आर० उत्तर पत्रक **(O.M.R. ANSWER SHEET)** पर ही दिये जाने हैं। उत्तर पत्रक में निर्धारित स्थान के अलावा अन्यत्र कहीं पर दिया गया उत्तर मान्य नहीं होगा।
5. ओ०एम०आर० उत्तर पत्रक **(O.M.R. ANSWER SHEET)** पर कुछ भी लिखने से पूर्व उसमें दिये गये सभी अनुदेशों को सावधानीपूर्वक पढ़ लिया जाय।
6. परीक्षा समाप्ति के उपरान्त परीक्षार्थी कक्ष निरीक्षक को अपनी प्रश्नपुस्तिका बुकलेट एवं ओ०एम०आर० शीट पृथक–पृथक उपलब्ध कराने के बाद ही परीक्षा कक्ष से प्रस्थान करें।
7. निगेटिव मार्किंग नहीं है।

महत्वपूर्ण : – **प्रश्नपुस्तिका खोलने पर प्रथमतः जॉच कर देख लें कि प्रश्नपुस्तिका के सभी पृष्ठ भलीभॉति छपे हुए हैं। यदि प्रश्नपुस्तिका में कोई कमी हो, तो कक्ष निरीक्षक को दिखाकर उसी सीरीज की दूसरी प्रश्नपुस्तिका प्राप्त कर लें।**

495

Rough Work / रफ कार्य

1. Collection of 8 bits is called :

   (A) Nibble

   (B) Word

   (C) Byte

   (D) Structure

2. Subtraction in intel 8085 is carried by :

   (A) 2's complement

   (B) 1's complement

   (C) 9's complement

   (D) Sign magnitude

3. What components are used in BUS design or data transfer between registers in CUP?

   (A) MUX, decoder

   (B) MUX, encoder

   (C) MUX, adder

   (D) DEMUX, decoder

4. Which of the following circuit is used to add 3 bits of data including a carry ?

   (A) Half adder

   (B) Full adder

   (C) Encoder

   (D) Register

5. Which of the following circuit is part of RAM and ROM ?

(A) Address decodes

(B) Encodes

(C) Multiplexer

(D) Demultiplexer

6. Which of following is true about CALL and RET instruction :

(A) Both are 3 byte instruction

(B) Both uses Push and POP operations respectively for their implementation

(C) Both transfer control conditionally

(D) None of the above

7. About PUSH and POP instruction in 8085, which is True :

(A) They are data transfer instructions

(B) They are two byte instruction

(C) They use top most memory location of stack

(D) They affect all flags

8. Among 5 interrupts of 8085 :

(A) TRAP is maskable interrupt

(B) TRAP is non-maskable interrupt & highest priority

(C) TRAP is having lowest priority

(D) None of the answer is correct

9. Which statement is true about LXI H, 2080 instech :

(A) Load H, L register with 20H, 80H respectively

(B) Load H, L register with 80H, 20H respectively

(C) It is a 2-byte instruction

(D) It uses direct addressing mode

10. Compare and complement opcodes in 8085 are _____ and _____ respectively.

(A) CMP, CMA

(B) CMA, CMP

(C) CM, CMA

(D) CP, CMA

11. RLC and RRC instructions means rotate accumulator :

(A) Left with carry, right with carry

(B) Left, right

(C) Right, left

(D) None of the above

12. INX B means :

(A) Increment register B

(B) Increment register pair BC

(C) Increment is register pair BD

(D) Increment is in Register mode

13. Which of the following is an instruction for Data Transfer from memory (pointed by H1pair) to microprocessor ?

(A) MOV M, R

(B) MOV R, M

(C) MVI R, M

(D) MVI M, R

14. JZ, JNZ instructions are used to :

(A) Check the end of loop execution

(B) Unconditionally jump

(C) execute based on carry flag

(D) None of the above

15. Which one is false ?

(A) INR and DCR affect content of given register

(B) INR and DCR affect all flags

(C) ADD, SUB instruction assume Accumulator as implied operand

(D) ADD, SUB do not affect the content of operand register

16. Which is true about data transfer instructions in 8085 ?

(A) They set all flags

(B) They do not affect any flags

(C) They do not affect source content

(D) In 08 H is a data transfer instruction

17. For program execution by the computer, the data and instructions are stored temporarily in :

(A) ROM

(B) RAM

(C) Control Unit

(D) Hard disk

18. In which of the following form, the computer stores data/instruction in memory ?

(A) Binary

(B) Hexadecimal

(C) Octal

(D) Decimal

19. In register mode, to specify any of 8 register, the no. of bits of used to specify a register is :

(A) 2

(B) 3

(C) 8

(D) 4

20. Which modes give easiest way to find operand ?

(A) implied, direct

(B) Implied, immediate

(C) Register indirect, relative

(D) Indexed, relative

21. Which is not true about assay processor ?

(A) It is a MIMD organized processor

(B) It can be attached to host computer

(C) It can be organized with multiple processing elements and multiple local memories

(D) These are highly specialized processor

22. Which is not true for a super computer ?

(A) It is commercial computer with vector instar and pipeline floating point arithmetic operation

(B) It is suitable as a general purpose computer

(C) It is very costly

(D) First super computer is CRAY-1

23. Choose the correct statement :

(A) Read and write control lines in CPU are bidirectional

(B) Read and write control lines in DMA controller are bidirectional

(C) Read, write control lines are unidirectional in DMA controller

(D) None of the above

24. Accumulator is a type of :

(A) Cache

(B) RAM

(C) MAR

(D) Register

25. Software method for implementing priority interrupt is called _____.

(A) Daily chaining

(B) DMA

(C) Polling

(D) Priority encoder

26. Hand shaking method :

(A) Used for synchronizing independent units communicating

(B) Uses strobe pulse

(C) Does not guarantee the receipt of message

(D) Used for data conversion

27. Input-output interface is used for :

(A) Signal conversion only

(B) Synchronization only

(C) Signal, data conversion, synchronization

(D) Data processing

28. What is not a possible register pair used in 8085 ?

(A) Accumulator and flag register

(B) Accumulator and B register

(C) Register D and E

(D) Register H and L

29. ADD M instruction uses_____ addressing mode.

(A) Register indirect

(B) Memory

(C) Direct

(D) Register

30. The CPI instruction :

(A) Compare Accumulator content and data byte

(B) Compare Accumulator and register

(C) Complement data bytes

(D) Complement accumulator

31. In the following instruction :

LXI H, 2050

MVI A, 20H

SUB M,

The size of each instruction written above are_____ respectively.

(A) 3, 2, 3 bytes

(B) 3, 2, 2 bytes

(C) 3,2, 1 bytes

(D) 2, 1, 3 bytes

32. For the following code, find the final value of Accumulator

MVI A, 33H

MVI B,78H

ADD B

CMA

ANI 52H

(A) 01 H

(B) 11 H

(C) 50 H

(D) 32 H

33. The content of accumulator after the executionof following instruction will be :

MVI A, L8 H

ORA A

RAL

(A) 6E H

(B) 91 H

(C) EF H

(D) ED H

34. The flag register in 8085 has_____ no. of flag bits.

(A) 4

(B) 5

(C) 6

(D) 3

35. Which of the following Pins of 8085 are used for DMA transfer_____?

(A) HOLD, HLDA

(B) INTR, IN

(C) RD, WR

(D) ALE, IO/$\overline{M}$

36. Which signal causes the microprocessor to terminate current activity ?

(A) Interrupt

(B) Reset

(C) Both

(D) HOLD

37. Which control signal is used for demultiplexing lower order address and data bus ?

(A) ALE

(B) HOLD

(C) RD

(D) IO/$\overline{M}$

38. ALE stands for (in 8085) :

(A) Address lower end

(B) Address latch end

(C) Address lower enable

(D) Address latch enable

39. The no of general purpose programmable register and memory pointer register are_____ , _____ respectively.

(A) 7, 2

(B) 8, 4

(C) 10, 2

(D) 8, 2

40. Which of the following is not a control signal in 8085 ?

(A) Read

(B) Write

(C) Reset

(D) ALE

41. Which of the following is used to store important info during subroutine call and interrupt ?

(A) Data register

(B) Queue

(C) Stack

(D) Address register

42. In 8085 microprocessor, what is size of stack pointer (SP) :

(A) 6 bit

(B) 16 bit

(C) 8 bit

(D) 32 bit

43. When 8085 performs the operation 7AH - A2H what will be the outcomes :

(A) Result = D8H, Cy =1, S= 0

(B) Result = D8H, Cy =0, S= 1

(C) Result = D8H, Cy =1, S= 1

(D) Result = D8H, Cy =0, S= 0

44. In 8085 microprocessor,which signal is used to delay Read, Write until a slow responding peripheral is ready to send or accept data :

(A) ALE

(B) READY

(C) HOLD

(D) INTR

45. Highest priority interrupt in 8085 is :

(A) RST 7.5

(B) RST 6.5

(C) TRAP

(D) INTR

46. The 8085 MP has :

(A) 8 bit data bus, 8 bit address bus

(B) 8 bit data bus, 16 bit address bus

(C) 16 bit data bus, 8 bit address bus

(D) 16 bit data bus, 8 bit data bus

47. Which of the following is a bulk data Transfer Technique ?

(A) Interrupt driven I/O

(B) DMA

(C) MIMD

(D) Subroutine call

48. For arithmetic pipeline (for add/ subtract), the following one the segments :

(i) Align the mantissa

(ii) Add/ subtract mantissa

(iii) Compare exponent

(iv) Normalize result

(A) (i), (ii), (iii), (iv)

(B) (iii), (i), (ii), (iv)

(C) (ii), (i), (iii), (iv)

(D) (iii), (ii), (i), (iv)

49. Which is not true about RISC ?

(A) It stands for reduced instruction set computer

(B) It uses microprogrammed control unit

(C) Memory access is limited to load and store instruction

(D) Easily decoded instruction format

50. Which of the following is a function of control unit :

(A) It performs logic operation

(B) It performs arithmetic operation

(C) It stores program

(D) It decodes the instructions of the program

51. Which of the following register collects the result of computation ?

(A) Instruction register

(B) Storage register

(C) MDR

(D) Accumulator

52. Which of the following circuit has 2^ninput lines and a single output lines ?

(A) Multiplexer

(B) Decodes

(C) Demultiplexer

(D) Encoder

53. A single bus system for data transfer between 8 register each of 16 bit, the number of multiplexers and size of each multiplexer are _____respectively.

(A) 16, 8×1

(B) 8, 16×1

(C) 16, 16×1

(D) 8, 8×1

54. Computer bus consists of _____.

(A) Accumulator

(B) Group of parallel lines

(C) Register

(D) Decodes

55. Which of the following is an elementary operation executed on data stored in register ?

(A) Macro operation

(B) Micro operation

(C) Stack operation

(D) Parallel operation

56. A system with an n-bit microprocessor has :

(A) n-bit data bus

(B) n-bit address bus

(C) n-bit program counter

(D) n-bit stack pointer

57. What does stack pointer hold ?

(A) Address of current instruction

(B) Address of current data

(C) Address of next instruction

(D) Address of top element of stack

58. Which is not True about program counter ?

(A) It is an instruction pointer

(B) It counts the statements in a program

(C) It has to be initialized first at the start of instruction cycle

(D) It stores the address of the next instruction to be executed

59. Which of the following is not a status bit :

(A) Unsigned bit

(B) Signed bit

(C) Carry bit

(D) Zero bit

60. What does SIMD stand for :

(A) Same instruction multiple data

(B) Simple instruction memory device

(C) Single instruction multiple data

(D) Single instruction multiple device

61. Which of the following informs a computer to perform a particular task ?

(A) Accumulator

(B) Instruction code

(C) Register

(D) Stack

62. Which of the following memory unit communicates directly with CPU ?

(A) Secondary memory

(B) RAM

(C) Auxiliary memory

(D) None of the above

63. In Booth's algorithm implementation, for multiplication of data represented with 2's complement form, What type of shift right operation is used :

(A) Logical

(B) Arithmetic

(C) Rotation with carry

(D) Circular

64. If an interrupt is caused by an instruction attempting to divide by zero, is said to create_____.

(A) External interrupt

(B) Internal interrupt

(C) Priority interrupt

(D) Software interrupt

65. In DMA Transfer, the required signals and addresses are given by_____.

(A) Processor

(B) Interrupt service routine

(C) DMA controller

(D) The program

66. The DMA transfer is initiated by :

(A) Operating system

(B) DMA controller

(C) Processor

(D) I/O device

67. Interrupts initiated by an instruction is called :

(A) Internal interrupt

(B) External interrupt

(C) Hardware interrupt

(D) Software interrupt

68. After the Interrupt service routine is returned_____ should be loaded again.

(A) Register contents

(B) Register contents and flag condition

(C) Flag condition

(D) Stack content

69. The Signal sent from processor to device after receiving an interrupt is :

(A) Service signal

(B) Return signal

(C) Interrupt

(D) Interrupt acknowledgement

70. The mode of Data transfer, which offer high speed I/O Transfer is :

(A) Programmed I/O

(B) Interrupt driven I/O

(C) Interrupt

(D) DMA

71. To check the readiness of the slower I/O device, the processor use :

(A) Buffer register

(B) Status flag

(C) Interrupt

(D) Exception

72. The microprocessor notifies a Read or Write operation by :

(A) Raising an interrupt signal

(B) Sending special control signal along BUS

(C) Enabling read/write bits of the device

(D) Adding extra bit to address

73. The place from which the return address is generated and used is :

(A) Stack

(B) RAM

(C) Heap

(D) ROM

74. The return address of the subroutine is pointer to by :

(A) Program counter value stored on stack

(B) Subroutine register

(C) Memory address register

(D) Stack pointer

75. Micro operation is _____.

(A) Complex operation on register

(B) Elementary operations done on register

(C) Complex instruction taking multiple clock cycles

(D) None of the above

76. _____converts the program written in assembly language to m/c language.

(A) Assembling

(B) Assembler

(C) Interpreter

(D) Compiler

77. The condition Flag Z is set to 1 indicate :

(A) Error in the operation

(B) Result is zero

(C) There is an error resulted

(D) Interrupt arise

78. When using branch instruction, the content of which register is altered first ?

(A) Instruction register

(B) Data register

(C) Program counter

(D) Accumulator

79. The steps in instruction cycle in proper order is :

(A) Fetch, decode, storage, execute

(B) Fetch, storage, decode, execute

(C) Fetch, decode, execute, storage

(D) Fetch, storage, execute

80. In a system which has 16 registers to do data processing,_____ bits are used to recognize the specified register.

(A) 16

(B) 12

(C) 4

(D) 6

81. The transfer of bulk of data is done (between memory and peripheral) by :

(A) Microcontroller

(B) DMA controller

(C) Arbitrator

(D) I/O processor

82. Which is true about LDA instruction (in 8085) ?

(A) Loads the content of Hard disk into a memory loc

(B) Loads the content of top of stack into accumulator

(C) Loads the content of memory location to accumulator

(D) Loads the content of memory to stack

83. The type of memory assignment used in Intel Processor is _____.

(A) Big Endian

(B) Little Endian

(C) Medium Endian

(D) Small Endian

84. If a system is 32 bit machine, then the length of each word is :

(A) 4 byte

(B) 8 byte

(C) 12 byte

(D) 16 bit

85. A 16 bit address generates an address space of_____ locations.

(A) 16 K

(B) 64 K

(C) 4096

(D) 1024

86. The Addressing mode where the operand value is part of instruction is_____ addressing mode.

(A) Direct

(B) Immediate

(C) Relative

(D) Indirect

87. The addressing mode, which uses program counter and other info for effective address calculation is_____ addressing mode.

(A) Relative

(B) Direct

(C) Auto increment

(D) Implied

88. The addressing mode using the extra indirection pointer is called _____addressing mode.

(A) Relative

(B) Indexed

(C) Register

(D) Indirect

89. Find the correct statement about zero address instruction :

(A) Stack pointer given the effective address

(B) There is no operand in the instruction

(C) Effective address is zero

(D) None of the above

90. To Reduce speed mismatch between CPU registers and main memory,_____ is used.

(A) Heap

(B) Stack

(C) Cache

(D) High capacity RAM

91. CISC stands for :

(A) Complete instruction set computer

(B) Complex instruction set computer

(C) Complex instruction sequence computer

(D) Computer for integrated set computer

92. When docing repetitive task through Loop operation, the instructions are stored in_____ for efficiency.

(A) Register

(B) Cache

(C) Heap

(D) Stack

93. A processor performingfetch or decode of different instructions during the execution of another instruction is called :

(A) Pipelining

(B) Superscalar

(C) Array Processor

(D) Vector Processor

94. During the instruction cycle for execution of an instruction, which register gets initialized first :

(A) MDR

(B) PC

(C) IR

(D) MAR

95. Instruction (for decoding)is stored in :

(A) PC

(B) Register

(C) IR

(D) MAR

96. The main use of single bus structure is :

(A) Cost effective connectivity and speed

(B) Cost effective connectivity and ease of attaching

(C) Fast data transfer

(D) None of the above

97. The I/O interface required to connect the I/O device to the bus has :

(A) Address decodes, register, control circuit

(B) Control circuit and register

(C) Register only

(D) Control circuit only

98. The ALU uses_____ to store the intermediate results.

(A) Register

(B) RAM

(C) Accumulator

(D) Stack

99. The extremely fast, small RAM are called as :

(A) Heap

(B) Cache

(C) Stack

(D) Accumulator

100. According to Von Neumann architecture, for computer_____ is/are stored in main memory.

(A) Data only

(B) Programs only

(C) Data and programs

(D) None of the above

******

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