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प्रश्नपुस्तिका क्रमांक
Question Booklet No.

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प्रश्नपुस्तिका सीरीज
Question Booklet Series
A

M.Sc (Electronics) Third Semester, Examination, February/March-2022
ELC-302(N)
IC Technology and VLSI Design

Time : 1:30 Hours **Maximum Marks-100**

जब तक कहा न जाय, इस प्रश्नपुस्तिका को न खोलें

निर्देश : –

1. परीक्षार्थी अपने अनुक्रमांक, विषय एवं प्रश्नपुस्तिका की सीरीज का विवरण यथास्थान सही– सही भरें, अन्यथा मूल्यांकन में किसी भी प्रकार की विसंगति की दशा में उसकी जिम्मेदारी स्वयं परीक्षार्थी की होगी।
2. **इस प्रश्नपुस्तिका में 100 प्रश्न हैं, जिनमे से केवल 75 प्रश्नों के उत्तर परीक्षार्थियों द्वारा दिये जाने है। प्रत्येक प्रश्न के चार वैकल्पिक उत्तर प्रश्न के नीचे दिये गये हैं। इन चारों में से केवल एक ही उत्तर सही है। जिस उत्तर को आप सही या सबसे उचित समझते हैं, अपने उत्तर पत्रक (O.M.R. ANSWER SHEET)में उसके अक्षर वाले वृत्त को काले या नीले बाल प्वांइट पेन से पूरा भर दें। यदि किसी परीक्षार्थी द्वारा निर्धारित प्रश्नों से अधिक प्रश्नों के उत्तर दिये जाते हैं तो उसके द्वारा हल किये गये प्रथमतः यथा निर्दिष्ट प्रश्नोत्तरों का ही मूल्यांकन किया जायेगा।**
3. प्रत्येक प्रश्न के अंक समान हैं। आप के जितने उत्तर सही होंगे, उन्हीं के अनुसार अंक प्रदान किये जायेंगे।
4. सभी उत्तर केवल ओ०एम०आर० उत्तर पत्रक **(O.M.R. ANSWER SHEET)** पर ही दिये जाने हैं। उत्तर पत्रक में निर्धारित स्थान के अलावा अन्यत्र कहीं पर दिया गया उत्तर मान्य नहीं होगा।
5. ओ०एम०आर० उत्तर पत्रक **(O.M.R. ANSWER SHEET)** पर कुछ भी लिखने से पूर्व उसमें दिये गये सभी अनुदेशों को सावधानीपूर्वक पढ़ लिया जाय।
6. परीक्षा समाप्ति के उपरान्त परीक्षार्थी कक्ष निरीक्षक को अपनी प्रश्नपुस्तिका बुकलेट एवं ओ०एम०आर० शीट पृथक–पृथक उपलब्ध कराने के बाद ही परीक्षा कक्ष से प्रस्थान करें।
7. निगेटिव मार्किंग नहीं है।

महत्वपूर्ण : – **प्रश्नपुस्तिका खोलने पर प्रथमतः जॉच कर देख लें कि प्रश्नपुस्तिका के सभी पृष्ठ भलीभॉति छपे हुए हैं। यदि प्रश्नपुस्तिका में कोई कमी हो, तो कक्ष निरीक्षक को दिखाकर उसी सीरीज की दूसरी प्रश्नपुस्तिका प्राप्त कर लें।**

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1. Which of the following material is used to make IC?

   (A) Germanium

   (B) Silicon

   (C) Boron Nitride

   (D) Copper

2. NMOS fabrication process is carried out in:

   (A) Thin wafer of a single crystal

   (B) Thin wafer of multiple crystals

   (C) Thick wafer of a single crystal

   (D) Thick wafer of multiple crystals

3. Which of the following components are not fabricated on IC?

   (A) Transistors

   (B) Resistors

   (C) Diodes

   (D) Transformers

4. The interconnections are made during _____.

   (A) Emitter diffusion process

   (B) Photolithography process

   (C) Epitaxial growth

   (D) Metallization process

5. _____ architecture is used to design VLSI.

   (A) System on a device

   (B) Single open circuit

   (C) System on a chip

   (D) System on a circuit

6. After placing the mask over the photoresist the wafer is subjected to _____.

(A) UV rays

(B) Visible light

(C) Infrared rays

(D) All of these.

7. MOSFET is a _____ controlled device:

(A) Current

(B) Voltage

(C) Resistance

(D) Impedance

8. How the aluminium film coating is carried out in metallization process?

(A) Heating and pouring aluminium in required place.

(B) Aluminium is vacuum evaporated and then condensed

(C) Placing the aluminium in required place and then heating it using tungsten

(D) None of the mentioned

9. The advantage of Multi-emitter transistor is:

(A) To reduce fabrication steps

(B) to save chip area

(C) To lower design consideration

(D) To provide linear output

10. The process involved in photolithography is:

(A) Making of a photographic mask only

(B) Photo etching

(C) Both photo etching and making of photographic mask

(D) None of the mentioned

11. Which type of etching process is preferred to make the photoresist immune to etchants?

(A) None of the mentioned

(B) Wet etching

(C) Plasma etching

(D) Chemical etching

12. If n-transistor conducts and has large voltage between source and drain, then it is said to be in_____ region.

(A) Linear

(B) Saturation

(C) Cut-off

(D) High impedance

13. Which insulating layer used in fabrication of MOSFET?

(A) Aluminium oxide

(B) Silicon Nitride

(C) Silicon dioxide

(D) None

14. What is the advantage of using Surface Mount Technology (SMD)?

(A) High speed

(B) Low power consumption

(C) Reduces heat dissipation in components

(D) Use leaded or leadless components

15. Which of the following is added as an impurity to p-type material in diffusion process?

(A) Phosphorous pentaoxide (P_2O_5)

(B) Phosphorous oxychloride ($POCl_3$)

(C) Boron oxide (B_2O_3)

(D) None of the mentioned

16. Which component is not used as an impurity in diffusion process?

(A) Phosphorous

(B) Boron chloride

(C) Phosphorous pentaoxide

(D) Boron oxide

17. Transconductance gives the relationship between _____.

(A) Input current and output voltage

(B) Output current and input voltage

(C) Input current and input voltage

(D) Output current and output voltage

18. Switching speed of a MOS device depends on:

(A) Gate voltage above a threshold

(B) Carrier mobility

(C) Length channel

(D) All of the mentioned

19. CMOS inverter has _____ output impedance.

(A) Low

(B) High

(C) Very high

(D) None of the mentioned

20. Gallium is produced as a byproduct of:

(A) Aluminium production process

(B) Sulphur production process

(C) Nitrogen production process

(D) Oxygen production process

21. Channel length modulation effect come after:

(A) Pinch-off

(B) Saturation effect

(C) Drain source voltage

(D) None

22. What is the advantage of using Ion implantation process?

(A) Lateral spreading is more

(B) Performed at high temperature

(C) Beam current controlled from outside

(D) Performed at low temperature

23. Oxidation is used for:

(A) Isolation

(B) Doping

(C) Interconnection

(D) None of the above

24. Doping means:

(A) Addition of impurity material in semiconductor band structure

(B) Removing of impurity material in semiconductor band structure

(C) Cleaning the surface

(D) None of the above

25. The transistors used in BiCMOS are _____.

(A) BJT

(B) MOSFET

(C) Both BJT and MOSFETs

(D) JFET

26. The pinch-off voltage of JFET is 5.0 volts. Its cut-off voltage is:

(A) 2.5 V

(B) 5.0 V

(C) $(5.0)^{1/2}$ V

(D) $(5.0)^{3/2}$ V

27. Inter-electrode capacitances in an FET are of the order of:

(A) 1pF

(B) 100 pF

(C) 0.1 μF

(D) 1 μF

28. The probability that an electron in a metal occupies the Fermi-level, at any temperature (>OK) is:

(A) 0

(B) 1

(C) 0.5

(D) None of the above

29. The width of the depletion region is:

(A) Independent of doping

(B) Inversely proportional to doping

(C) Directly proportional to doping

(D) One of the above

30. What are the advantages of BiCMOS?

(A) Higher gain

(B) High frequency characteristics

(C) Better noise characteristics

(D) All of the mentioned

31. For an enhancement-type MOSFET the output V-I characteristic of has:

(A) Only a saturation region

(B) An ohmic region at low voltage value followed by a saturation region at higher voltages

(C) An ohmic region at large voltage values preceded by a saturation region lower voltage

(D) Only an ohmic region

32. When a diode is forward-biased, the recombination of free electron and holes may produce:

(A) Heat

(B) Light

(C) Radiation

(D) All of the above

33. The LED is usually made of materials like:

(A) GaAs

(B) Si

(C) GeAs

(D) None of the above

34. Doping concentration of BJT is high in the:

(A) Collector region

(B) Base region

(C) Emitter region

(D) None of the above

35. The threshold voltage of an n-channel enhancement mode MOSFET is 0.5 V. When the device is biased at a gate voltage of 3 V. Pinch-off would occur at a drain voltage of:

(A) 2.5 V

(B) 0.5 V

(C) 3.0 V

(D) 3.5 V

36. The main factor, which differentiates a D-MOSFET from an E-MOSFET, in the absence of:

(A) p-n Junction

(B) Channel

(C) Electrons

(D) Insulated gate

37. n-channel FET's are superior to p-channelFET's because:

(A) Mobility of electrons is smaller than that of holes

(B) They have high switching time

(C) Mobility of electrons is greater than that of holes

(D) They consume less power

38. The drain current in JFET is controlled by:

(A) Channel resistance

(B) Voltage drop across channel

(C) Reverse-bias at the gate

(D) Depletion regions

39. FET has offset voltage of about:
    (A) Zero
    (B) 0.2 V
    (C) 0.5 V
    (D) 1 V
40. Stick diagrams are those which convey layer information through?
    (A) Thickness
    (B) Color
    (C) Shapes
    (D) Layers
41. An n-channel JEET has I_{DSS}= 2 mA and V_p = – 4 v. Its transconductance g_m (in milli mho) for an applied gate-to-source voltage V_{Gs} of – 2 V is:
    (A) –8 V
    (B) 0.5 V
    (C) 0.75 V
    (D) –2 V
42. The threshold voltage of an n-channel MOSFET can be increased by:
    (A) Reducing the channel dopant concentration.
    (B) Reducing the channel length
    (C) Reducing the gate oxide thickness.
    (D) Increasing the channel dopant concentration.
43. Find the application areas, where Schottky diode can be used?
    (A) Radio frequency
    (B) Power rectifier
    (C) Clamping diode
    (D) All of the mentioned
44. Metallization is used for:
    (A) Protection
    (B) Interconnection
    (C) Packaging
    (D) None of the above

45. Which color is used for n-diffusion in stick diagrams?
    (A) Red
    (B) Blue
    (C) Green
    (D) Yellow
46. What is the crystal structure of silicon?
    (A) Face Centred Cubic
    (B) Body Centred Cubic
    (C) Diamond
    (D) Hexagonal
47. Packaging is used for:
    (A) Protection
    (B) Safety
    (C) Both (A) & (B)
    (D) None of the above
48. Optical masking is used:
    (A) Etching
    (B) Protection
    (C) Pattern transfer
    (D) Cleaning
49. Etching is used for:
    (A) Protection
    (B) Interconnection
    (C) Selective removal of the unwanted surface
    (D) None
50. Inductor design in an IC:
    (A) Is possible with discrete components
    (B) Is not possible
    (C) Is possible
    (D) None of the above

51. As die size shrinks, the complexity of making the photomasks _____.

(A) Increases

(B) Decreases

(C) Remains the same

(D) Cannot be determined

52. _____ is used in logic design of VLSI.

(A) LIFO

(B) FIFO

(C) FILO

(D) LILO

53. Wafers properties depend upon the _____ of crystalline structures.

(A) Orientation

(B) Concentrations of impurity

(C) Presence of various impurities

(D) All the above

54. What is the second step in the IC fabrication?

(A) Doping

(B) Oxidation

(C) Metallization

(D) Orientation

55. Oxidation in silicon can be occurred by raising _____.

(A) Pressure

(B) Humidity

(C) Temperature

(D) Volume

56. Which is used as the dielectric layer in MOS Capacitor?

(A) Silicon Nitride (Si3N4)

(B) Aluminium oxide (Al203)

(C) Tantalum oxide (Ta2O5)

(D) All of the mentioned

57. _____ MOSFETs are always ON initially.

(A) Enhancement

(B) Depletion

(C) Both (A) & (B)

(D) None of the above

58. Which color is used for polysilicon?

(A) Brown

(B) Red

(C) White

(D) Orange

59. Why MOSFET is preferred over BJT in IC components?

(A) MOSFET has low packing density

(B) MOSFET has medium packing density

(C) MOSFET has high packing density

(D) MOSFET has no packing density

60. Inverters are essential for _____.

(A) NAND gates

(B) NOR gates

(C) Sequential circuits

(D) All of the mentioned

61. What is pinch off voltage?

(A) A voltage at which the current gets pinched to zero

(B) Maximum voltage a FET can withstand

(C) Current amplification factor/voltage gain

(D) Minimum voltage required to turn on the FET

62. Which is the software used in VLSI?

(A) Xilinx

(B) Cadence

(C) LOON

(D) All of the above

63. Design rules does not specify _____.

(A) Linewidths

(B) Separations

(C) Extensions

(D) Colours

64. The width of n-diffusion and p-diffusion layer should be?

(A) 3λ

(B) 2λ

(C) λ

(D) 4λ

65. The _____ is used to reduce the resistivity of poly silicon.

(A) Photo resist

(B) Etching

(C) Doping impurities

(D) None of the mentioned

66. Surface mobility depends on:

(A) Channel length

(B) Effect gate Voltage

(C) Effect drain Voltage

(D) None

67. The leakage current across a pn junction is due to:

(A) Minority carriers

(B) Majority carriers

(C) Junction capacitance

(D) None

68. Electrical charge flows from _____.

(A) Source to drain

(B) Drain to source

(C) Source to ground

(D) Source to gate

69. In n channel MOSFET _____ is constant.

(A) Channel length

(B) Channel width

(C) Channel depth

(D) Channel concentration

70. To grow $1\mu m$ thick SiO2 layer on the Si wafer which of the process is preferabel?

(A) Both dry and wet oxidation are equally preferable

(B) CVD

(C) Wet Oxidation

(D) Dry oxidation

71. Which color is used for contact areas?

(A) Red

(B) Brown

(C) Black

(D) Blue

72. Which method is most suitable for silicon crystal growth in silicon wafer preparation?

(A) Float zone process

(B) Bridgeman-Stockbarger method

(C) Czochralski crystal growth process

(D) Laser heated pedestal growth

73. A hole in a semiconductor is defined as_____.

(A) A free electron

(B) The incomplete part of an electron pair bond

(C) A free proton

(D) None

74. What is the condition for saturation?

(A) $V_{gs} = V_{ds}$

(B) $V_{ds} = V_{gs} - V_t$

(C) $V_{gs} = V_{ds} - V_t$

(D) $V_{ds} > V_{gs} - V_t$

75. A semiconductor has generally _____ valence electrons.

(A) 2

(B) 3

(C) 4

(D) 6

76. When a junction transistor is operated under saturation conditions:

(A) Both the CB and EB junction are forward biased

(B) The CB junction is forward biased but EB junction is reverse biased

(C) The CB junction is reverse biased but EB junction is forward biased

(D) None

77. Concentration gradient refers to:

(A) Change of concentration with respect to time

(B) Change of concentration with respect to space

(C) Change of concentration with respect to temperature

(D) None of the mentioned

78. The spacing of interconnect is scaled by:

(A) α

(B) $1/\alpha$

(C) α^2

(D) $1/\alpha^2$

79. NMOS is _____.

(A) Donor doped

(B) Acceptor doped

(C) All of the mentioned

(D) None of the mentioned

80. What are the types of MOSFET devices available?

(A) P-type enhancement type MOSFET

(B) N-type enhancement type MOSFET

(C) Depletion type MOSFET

(D) All of the mentioned

81. P-well is created on _____.

(A) p substrate

(B) n substrate

(C) p & n substrate

(D) None of the mentioned

82. Gallium arsenide is made up of:

(A) Single element

(B) Compound of two elements

(C) Compound of three elements

(D) Compound of four elements

83. Which has low power dissipation?

(A) NMOS

(B) PMOS

(C) BJT

(D) CMOS

84. The saturation drain current I_{DS} is an FET equals:

(A) $I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$

(B) $I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)$

(C) $I_{DSS}\left(\frac{\sqrt{V_{GS}}}{V_p}\right)$

(D) $I_{DSS}^2\left(\frac{V_{GS}}{V_p}\right)$

85. MOSFET is used as _____.

(A) Current source

(B) Voltage source

(C) Buffer

(D) Divider

86. The mobility is given by:

(A) $\mu = V_0/E_0$

(B) $\mu = V_0^2/E_0$

(C) $\mu = V_0/E_0^2$

(D) None of the above

87. Why MOSFET is preferred over BJT in IC components?

(A) It has low packing density

(B) It has medium packing density

(C) It has high packing density

(D) It has no packing density

88. What is the advantage of using Czochralski & Bridgman method?

(A) Gives small crystals

(B) High tech apparatus

(C) Rapid growth rates

(D) Uses Plasma torch

89. Which of the following is a property of amorphous solids?

(A) Sharp melting point

(B) Isotropy

(C) Long range order

(D) Definite heat of Fusion

90. In BiCMOS inverter, the BJT used are _____.

(A) Only npn BJT

(B) Only Pnp BJT

(C) Both npn and pnp BJT

(D) Multi emitter npn BJT

91. Multipliers are built using:

(A) Binary adders

(B) Binary subtractors

(C) Dividers

(D) Multiplexers

92. Co-ordination number of a crystalline solid is:

(A) Number of particles in the unit cell

(B) Number of nearest neighbours of a particle

(C) Number of octahedral voids in a unit cell

(D) Number of tetrahedral voids in a unit cell

93. Which occupies lesser area?

(A) NMOS

(B) PMOS

(C) CMOS

(D) BiCMOS

94. _____layer should be over _____ layer used in stick diagram representation:

(A) ntype, polysilicon

(B) polysilicon, ntype

(C) ptype, ntype

(D) ntype, ptype

95. A sequential circuit contains combinational logic and storage elements in:

(A) Output node

(B) Feedback path

(C) Input node

(D) Feed forward path

96. Bipolar transistors are _____ than field effect transistor.

(A) Less sensitive and slower

(B) More sensitive and slower

(C) More sensitive and faster

(D) Less sensitive and faster

97. In CMOS NAND gate, PMOS is connected in:

(A) Series

(B) Parallel

(C) Random

(D) None

98. In NMOS device, gate material could be _____.

(A) Silicon

(B) Boron

(C) Polysilicon

(D) Phosphorus

99. CMOS technology is used in developing which of the following?

(A) Microprocessors

(B) Microcontrollers

(C) Digital logic circuits

(D) All of the mentioned

100. ASIC stands for _____.

(A) Application standard of integrated circuits

(B) Application-specific intercommunication circuit

(C) Application-specific integrated circuit

(D) American standard integrated circuit

******

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