Chhatrapati Shahu Ji Maharaj University, Kanpur

Answer Script Details
Barcode 10293269

Roll No. 23071002365
Total Mark 46/75.00

Exam BACHELOR OF COMPUTER APPLICATIONS_ODD EXA
Subject BCA3004 - DIGITAL ELECTRONICS AND COMPUTER

Question wise Mark Summary

Q.No	Mark	Q.No	Mark	Q.No	Mark	Q.No	Mark
1A	3/5						
1B	3/5						
1C	3/5						
1D	3/5						
1E	3/5						
1F	3/5						
1G	3/5						
1H	3/5						
1I	3/5						
2	NA/15						
3	9/15						
4	NA/15						
5	NA/15						
6	NA/15						
7	NA/15						
8	NA/15						
9	10/15						

Chhatrapati Shahu Ji Maharaj University
Kanpur, Uttar Pradesh

Date of Exam : 04/01/25 Shift : Afternoon Room No. G-12
Paper Code : BCA-3004 Subject : Digital Electronics and Computer Organization Year/Sem. III rd Sem
Name of Candidate : Khyati Trivedi
Roll No. 2307100236 5

COE Facsimile

Signature of Invigilator

Signature of Candidate

PART-II

MARKS OBTAINED										
Q.	1	2	3	4	5	6	7	8	9	10
(a)										
(b)										
(c)										
(d)										
(e)										
(f)										
(g)										
(h)										
(i)										
(j)										
Total										
Total Marks in Figures									Max. Marks	
Total Marks in Words										

Paper Code

Signature of Evaluator

Course Bachelor of Computer Application

Session 2024-2027 Year/Semester III rd Sem

Subject Digital Electronics & Computer Organization

Paper Code BCA3004

Exam Date 04/01/2025

Name of Candidate HYATI TRIVEDI

Father's Name K TRIVEDI

महाविद्यालय का कोड College Code: KN162

परीक्षा केन्द्र का कोड Exam Centre Code: KN162

परीक्षा का प्रकार Type of Exam: Regular ● Ex. Student ○ Private ○ Re-Exam other/Back paper Exam ○

ANSWER BOOKLET NO. 10293269

BCA3004

Paper Code

नामांकन संख्या Enrollment Number: CSJMA23000129517

परीक्षार्थी अनुक्रमांक संख्या Candidate's Roll Number: 2307100236 5

पेपर कोड Paper Code: 3004

Khyati Trivedi

Signature of Candidate

Signature of Invigilator

C.S. Facsimile

COE Facsimile

नोट : 1. परीक्षार्थी को निर्देशित किया जाता है कि आवरण पृष्ठ के पृष्ठ भाग पर अंकित सभी निर्देशों को सावधानी पूर्वक पढ़ें।
2. बॉक्स में भरी जाने वाली प्रविष्टियाँ काली स्याही से भरी जायें। 3. पोथी को काले या नीले बॉलपेन से भरा जायें।

INSTRUCTIONS TO THE CANDIDATE FOR FILLING PART-I

1. Read the instructions carefully given on the answer script and admit card.
2. Write Date of Exam, Shift, Paper Code & Name of Subject Correctly.
3. Write Name & Roll No. Correctly.
4. Write Semester & Branch Correctly.

INSTRUCTIONS TO THE CANDIDATE FOR FILLING PART-III

1. Use blue or black ball point pen for writing alphabets & numerals in ☐ Boxes.
2. Carefully study the example before you start marking.
3. As shown in the example below blacken the circles completely.

Correct method: ① ● ③ ④

Incorrect method: ✓ ✗ ◉ ⓿

4. Make no Stray marks on this sheet.
5. **DO NOT WRITE OR MARK ON THE BAR CODE.**

IN ORDER TO AVOID UFM (UNFAIR MEANS) :

1. The Roll No. and Answer Book no. found elsewhere or any other symbol found in the answer book will be treated as unfair means.
2. Any tempering of Bar Code and Booklet no shall be treated as Unfair Means.
3. Do Not bring the materials like slip of paper/mobile/digital diaries/ study material/ revision notes in examination hall. Possession of the mobiles/ digital diaries/ electronic watch and any other electronic gadget except memory less scientific calculator shall be considered as UFM case.
4. Do not keep or paste currency note in answer script it shall be consider as UFM.

अनुचित साधन से बचने हेतु:

1. उत्तर पुस्तिका के निर्देशित स्थान को छोड़कर अनुक्रमांक एवं उत्तरपुस्तिका का क्रमांक कहीं और न लिखें तथा कोई भी चिन्ह न बनायें क्योंकि यह अनुचित साधन प्रयोग की परिधि में आता है।
2. उत्तर पुस्तिका के बारकोड अथवा उत्तर पुस्तिका संख्या पर छेड़ करने पर अनुचित साधन प्रयोग माना जायेगा।
3. परीक्षा कक्ष में निम्न वस्तुएं साथ न लायें, जैसे लिखे हुए कागज के टुकड़े, मोबाईल, डिजिटल डायरी, कोपी, पुस्तक यह सभी वस्तुएं जो अनुचित साधन के अन्तर्गत आती है। केवल संबंधित प्रश्नपत्र में ही मेमोरी लेस साइंटफिक केलकुलेटर ले जाने की अनुमन्यता होगी।
4. उत्तर पुस्तिकाओं में रूपये न रखें न ही उत्तर पुस्तिका में चिपकायें। ऐसा करना अनुचित साधन प्रयोग की परिधि में आता है।

परीक्षार्थी के लिए निर्देश

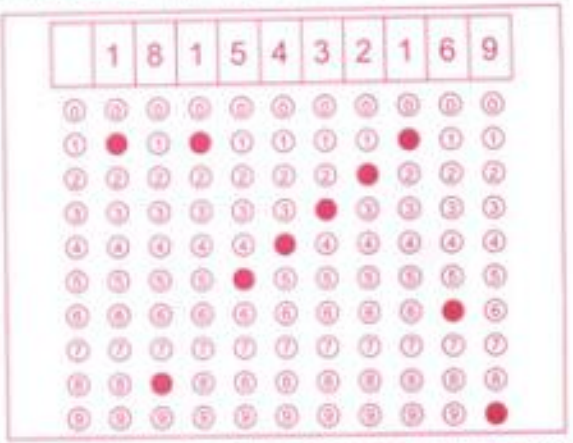
1. प्रवेश पत्र एवं उत्तर पुस्तिका पर दिये गये निर्देशों को ध्यान से पढ़ें।
2. कवर पृष्ठ के दूसरी तरफ कुछ न लिखें।
3. उत्तर पुस्तिका के पृष्ठों पर दोनों तरफ लिखें।
4. प्रश्न पत्र पर अपने अनुक्रमांक के अतिरिक्त कुछ न लिखें।
5. प्रश्न पत्र कोड एवं प्रश्न पत्र कोड सावधानी पूर्वक लिखें।
6. अपनी स्थिति स्पष्ट लिखें।
7. उत्तर पुस्तिका के पृष्ठों की संख्या देखें। अगर उत्तर पुस्तिका में पृष्ठ (1–24) से कम है या फटे हुए है, तो परीक्षा शुरू होने के पूर्व दूसरी उत्तर पुस्तिका ले लें।
8. प्रश्नपत्र को देख, यदि प्रश्नपत्र के विषय कोड, विषय का नाम तथा प्रश्न में कोई त्रुटि है तो उसके परीक्षा शुरू होने के 30 मिनट के अन्दर कक्ष निरीक्षक को तत्काल सूचित करें, उसके बाद विश्वविद्यालय द्वारा कोई कार्यवाही नहीं की जायेगी।
9. प्रश्नों के उत्तर लिखने के लिये पेंसिल का प्रयोग न करें।
10. B कोपी या अतिरिक्त ग्राफ नहीं दिया जायेगा।

INSTRUCTIONS TO THE CANDIDATE

1. Read the instructions carefully given on the Question Pape Admit Card & Answer Script.
2. Do not write anything on back side of the cover page.
3. Write on both sides of pages of answer book.
4. Do not write anything on question paper except Roll Number.
5. Write Paper Code & Question Paper Id carefully.
6. CHECK the number of pages (1-32) or any other kind of damag in your answer script, if found than change the answer scri immediately before the commencement of examination.
7. CHECK the Question Paper for any kind of discrepancy e Subject Code, Subject Name and Question of the Questi Paper during first THIRTY MINUTES of the commencement the exam, so that it can be corrected in TIME. After that r corrections shall be entertained by the university.
8. Do not use pencil for answering the question.
9. Write status correctly e.g. those appearing in carry over pape should fill in status as Carry Over. Those appearing as F Students should fill in status as ex.
10. No supplementary answer book & graph paper will be provided

INSTRUCTIONS TO THE CANDIDATE FOR FILLING PART-IV

1. Use blue or black ball point pen for writing alphabets & numbera in ☐ Boxes.
2. Use blue or black ball point pen for filling the circles.



Note - If your Roll No. is of 10 digits. Please leave first three colu

Paper Code

01

Section-A

a. Minterm

- A minterm is a combination of boolean variables which are combined with AND (·) operator.
- Each variable in a minterm can exist in its real or complemented state.
- A minterm is used in a formation of SOP (Sum of Product) Expression. In which the minterms are combined is (+) or operator.
- If there are two variables x and y the number of possible combinations of minterms = 2^n
  So there can be $2^2 = 4$ possible minterms $x'y'$, xy', $x'y$, xy.
- A minterm is formed when a function result = 1
- These are represented by m.
- For three variable a, b, c

a	b	c	Minterms		
0	0	0	m_0	$a'b'c'$	Total 8 combination
0	0	1	m_1	$a'b'c$	
0	1	0	m_2	$a'bc'$	
0	1	1	m_3	$a'bc$	
1	0	0	m_4	$ab'c'$	
1	0	1	m_5	$ab'c$	
1	1	0	m_6	abc'	
1	1	1	m_7	abc	

Maxterms:

- Maxterms are a combination of boolean variables in which the variables are combined using + OR operation.
- A maxterm is used for the formation of POS (product of sum) functions expressions.
- A maxterm is formed when a boolean function results to 0.
- In maxterms the complemented state is 1 and real state is 0.
- It is represented by M.
- For ~~two~~ n variables there can be 2^n combinations of maxterms therefore for 3 variables A, B, C.

A	B	C	Maxterms	
0	0	0	$a+b+c$	M_0
0	0	1	$a+b+\bar{c}$	M_1
0	1	0	$a+\bar{b}+c$	M_2
0	1	1	$a+\bar{b}+\bar{c}$	M_3
1	0	0	$\bar{a}+b+c$	M_4
1	0	1	$\bar{a}+b+\bar{c}$	M_5
1	1	0	$\bar{a}+\bar{b}+c$	M_6
1	1	1	$\bar{a}+\bar{b}+\bar{c}$	M_7

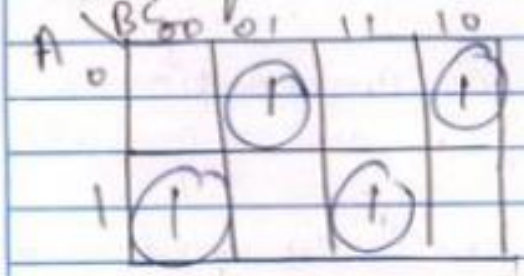
b. Full Adder

- A full Adder is a combinational circuit that has 3 inputs and 2 outputs.
- A full adder is used to add 3 binary bits at a time.
- For three inputs A, B, C it has two outputs which sum and carry. Therefore when we take the inputs it will store the addition of the input combination in the sum part. The least-significant bit of the result is stored in the sum and carry stores 1 if there is a carry and 0 if there is no carry.

Truth Table of Full Adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K Map for Sum



$f = f_1 + f_2 + f_3$

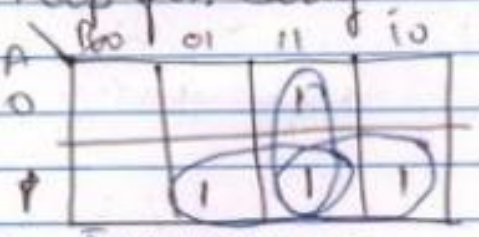
$f = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= \bar{A}(B \oplus C) + A(B \oplus C)'$ → because $(\overline{BC} + BC)' = (\overline{BC} \cdot \overline{BC})' = (\bar{B} + \bar{C} \cdot \bar{B} \cdot \bar{C})' = (\bar{B}\bar{B} + B\bar{C} + C\bar{B} + C\bar{C})' = (B\bar{C} + C\bar{B})' = (B \oplus C)'$

Sum = $A \oplus B \oplus C$

K Map for Carry



$f_1 = \bar{A}BC + ABC$ ✓

$f_2 = A\bar{B}C + ABC$

$f_3 = AB\bar{C} + ABC$

$f = f_1 + f_2 + f_3$

$= \bar{A}BC + ABC + A\bar{B}C + AB\bar{C}$

$= BC(A + \bar{A}) + A(\bar{B}C + C\bar{B})$

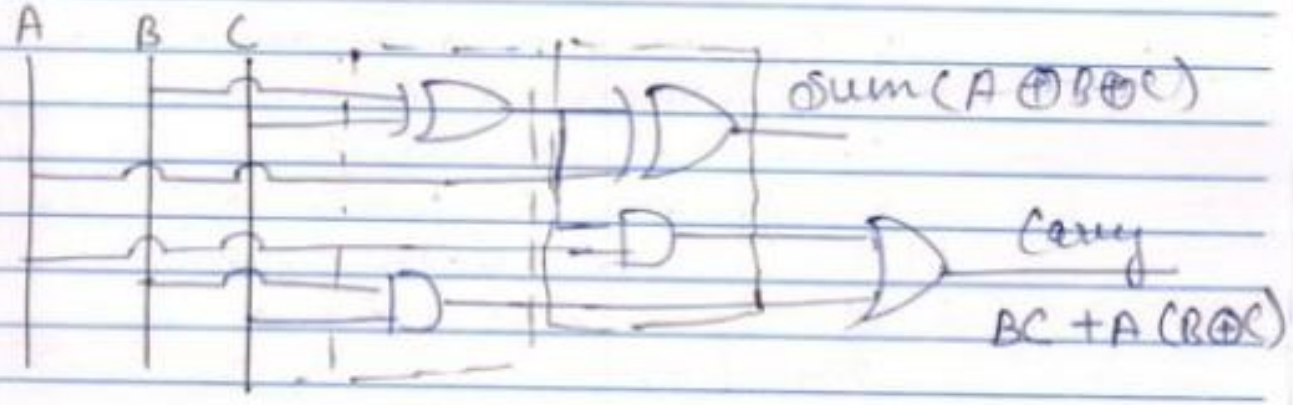
Carry = $BC + A(B \oplus C)$

(b) Gate representation

Paper Code

05

Gate Representation:



c. hexadecimal 2A to octal.

- We can convert a hexadecimal to octal by first changing it into decimal & then converting the resultant decimal to Octal.
  Hex → decimal → Octal
- Or we can also take out the binary of each digit of the hex & write its octal representation in a pair of 3.

$2A \rightarrow$ dec $\rightarrow$ octal

$2 \times 16^1 + A \times 16^0$

$2 \times 16 + 10 \times 16^0$

$32 + 10$

$(42)_{10} \rightarrow$?

8	42	2 ↑
8	05	5
	0	

$= (52)_8$

$(2A)_{16} = (52)_8$ Answer.

Hexadecimal to binary.

In order to convert a hexadecimal to binary we need to write the binary of each digit of the hex number & then write all the binaries sequentially shows the binary equivalent of that number.

$(2A)_h \rightarrow (?)_2$

(2) = 0010

A = 1010

$\boxed{(2A)_h = (0010\ 1010)_2}$

a. (Flip Flop)

- A Flip Flop is a sequential circuit that is used as a memory element in various sequential circuits.
- A Flip Flop is a bistable circuit which means that it can exist in two stable states which are 0 and 1.

- It is used to preserve the state of a sequential circuit for some amount of time. and then it returns the state as input in feedback to the sequential circuit.
- One flip flop can store only 1 bit of information and if we want to store multiple bits then we should use a series of flip flops.
- There are various types of flip flops which are used to digital counters, registers, control systems and perform binary arithmatic.
- There are total 4 types of flip flops.
  1. SR flip flop [Set Reset flip flop]
  2. J flip flop
  3. D flip flop [Delay flip flop]
  4. T flip flop
- A flip flop is made active by Triggering which can be level or edge.

⇒ Characteristic Table of SR flip flop

SR flip flop is a flip flop that stores the previous state only when both the input combination

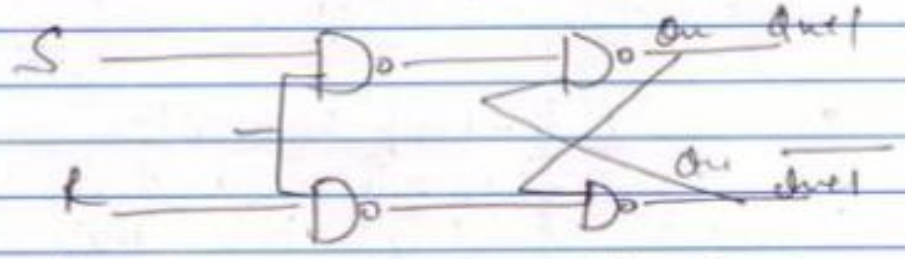
are two which means

S=0 R=0 ⇒ Output = Q_n (memory)

S=0 R=1 ⇒ Output = 0 (Reset)

S=1 R=0 ⇒ Output = 1 (Set)

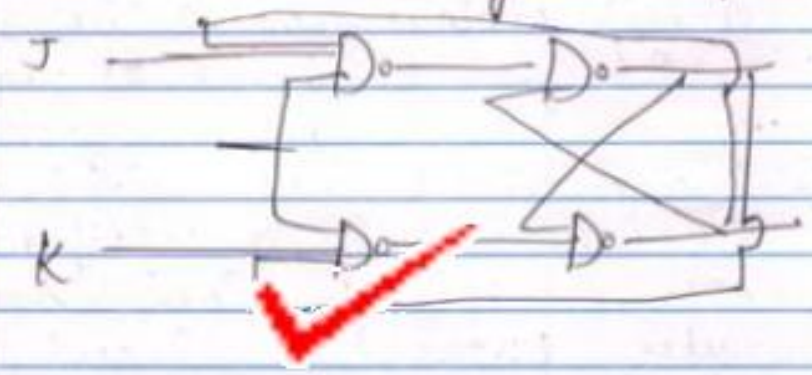
S=1 R=1 ⇒ Output = Invalid state



using this we draw the characteristic table

S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	0	0	1	memory
0	0	1	1	0	
0	1	0	0	1	Reset
0	1	1	0	1	
1	0	0	1	0	Set
1	0	1	1	0	
1	1	0	1	1	Invalid.
1	1	1	1	1	

⇒ Characteristic Table of JK Flip Flop



Here all case are same but the invalid case is removed and Toggle is introduced when $J=1$ $K=1$ Output = Toggle which means reverse of pr. cur. state.

J	K	Q_n	Q_{n+1}	$\bar{Q}_{n+1}$	
0	0	0	0	1	} memory
0	0	1	1	0	
0	1	0	0	1	} Reset
0	1	1	0	1	
1	0	0	1	0	} Set
1	0	1	1	0	
1	1	0	1	0	} Toggle.
1	1	1	0	1	

f° ...1.

If the memory given then it can be broken down as $2^n \times m$ bytes which means that in RAM there are n address lines and m data lines.

Memory = 4096 X 16 ✓

4096X16 can be written as - $2^{12} \times 16$

∴ no. of address line $= 2^n$

$= 2^{12}$

$\boxed{n = 12}$

and no. of data line = m

from

$2^{12} \times 16$

$m = 16$

∴

no. of data line = 16

no. of chip select = 2^{m-8}

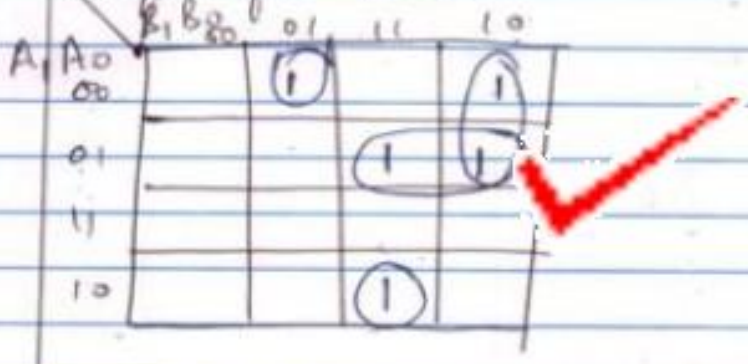
9

1. Truth Table for a 2 bit Comparator

A_1	A_0	B_1	B_0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	0	0	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

It is used to compare two bit number A & B & each digit is compared acc. to its position.

Output for $A < B$



$f_1 = \bar{A}_1 A_0 \bar{B}_1 B_0$

$f_2 = \bar{A}_1 \bar{A}_0 B_1 \bar{B}_0 + \bar{A}_1 A_0 B_1 \bar{B}_0$

$= \bar{A}_1 B_1 \bar{B}_0$

$f_3 = \bar{A} A_0 B B_0 + \bar{A} A_0 B \bar{B}_0$

$= \bar{A}_1 A_0 B_1$

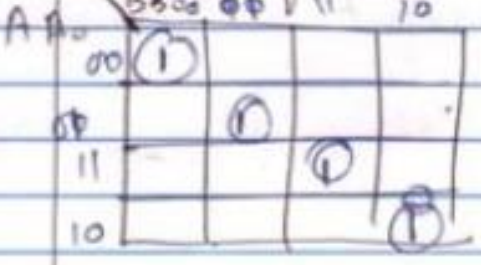
$f_4 = A_1 A_0 B B_0$

$F = \bar{A}_1 \bar{A}_0 \bar{B}_1 B_0 + \bar{A}_1 B_1 \bar{B}_0 + \bar{A}_1 A_0 B_1 + A_1 \bar{A}_0 B B_0$

$= \bar{A}_0 B_0 (\bar{A}_1 B_1 + A_1 B_1) + \bar{A}(B_1 \bar{B}_0 + A_0 \bar{A}_1 B_1 (\bar{B}_0 + A_0)$

$F = \bar{A}_0 B_0 (A \oplus B)' + \bar{A}_1 B_1$

Output for $A = B$



$f = \bar{A}\bar{A}_0 B\bar{B}_0 + \bar{A} A_0 \bar{B} B_0 + A A_0 B B_0 + A \bar{A}_0 B \bar{B}_0$

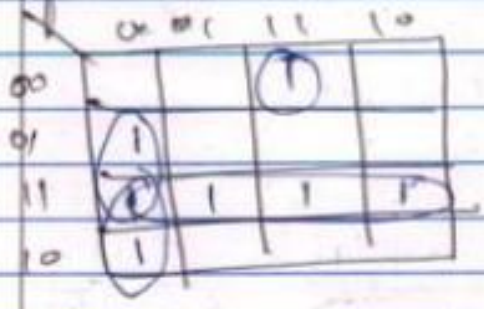
$= \bar{A}\bar{B}(\bar{A}_0 \bar{B}_0 + A_0 B_0) + AB(A_0 B_0 + \bar{A}_0 \bar{B}_0)$

$= \bar{A}\bar{B}(A_0 \oplus B_0)' + AB(A \oplus B_0)'$

$= \bar{A}\bar{B}(A \oplus B)' + AB(A \oplus B_0)$

$F = (A \oplus B)'$

for $A > B$



$F_1 = \bar{A}\bar{A}_0 B B_0$

$F_2 = \bar{A} A_0 \bar{B}\bar{B}_0 + A A_0 \bar{B}\bar{B}_0$

$= A\bar{B}\bar{B}_0$

$F_3 = A_1 B_1 B_0$

$F_4 = A A_0$

$F = \bar{A}\bar{A}_0 B B_0 + A_0 \bar{B}\bar{B}_0 + A_1 B_1 B_0 + A_1 A_0$

$= B_1 B_0 (\bar{A}_1\bar{A}_0 + A_1) + A_0 (\bar{B}\bar{B}_0 + B_1)$

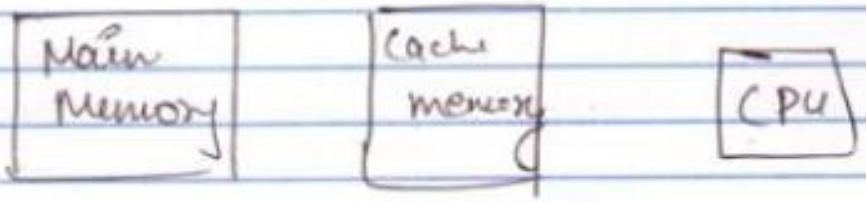
$= A_1\bar{B}_1 + A_0\bar{B}_1(A_1 \oplus B_1)'$

g. Advantages of Cache Memory Organization

- Cache Memory is placed between the main memory & the CPU therfore it is very quickly accessed by the CPU!
- A cache memory is volatile therfore we can swap in and swap out pages

and therefore we can accomodate a very large amount of data into cache memory.

- Cache memory is very versatile & it can carry multiple processes inside it can be carried & then the CPU can also perform Multiprogramming.
- Cache memory is the first memory which is checked by the CPU so it can provide frequent information to the CPU.



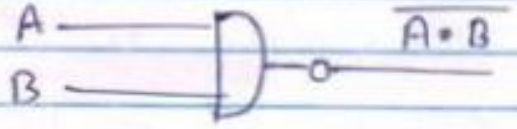
- Cache memory can also extend the concept of virtual memory where there is a illusion given that all the programs are in main memory but actually less pages of each process are there in the cache memory.
- A cache memory also has page replacement algorithms that can help efficient allocation & de-

allocation of Memory to processes.

- Cache memory has SRAM where data is loaded ~~eq~~ statically so it does not needs to be refreshed again & again & it can retain data for large amount of time.

b). De Morgan's Theorem
First law:

i) $\overline{A \cdot B} = \bar{A} + \bar{B}$



This can also be equal to

$\bar{A} + \bar{B}$

For $A = 1$, $B = 0$

$\overline{A \cdot B} = \overline{1 \cdot 0} = \overline{0} = 1$

$\bar{A} + \bar{B} = 0 + 1 = 1$

which are equal Hence proved.

Second Law

→ $(A+B)' = A' \cdot B'$

For two variables A and B when

$A = 0$

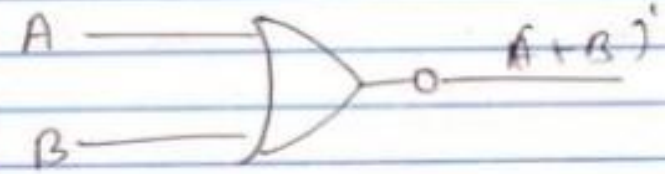
$B = 1$

$(A+B)' = (0+1)' = (1)' = 0$

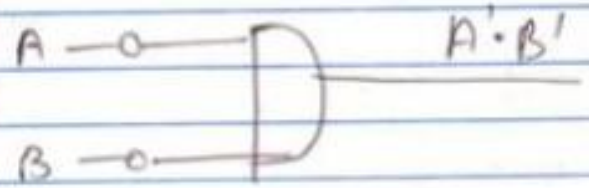
$A' \cdot B' = 0' \cdot 1' = 1 \cdot 0 = 0$

which are equal ⇒ hence proved.

10

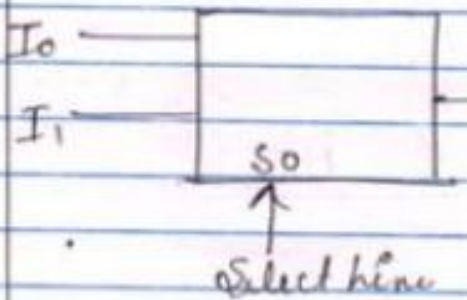


$(A+B)' = A' \cdot B'$

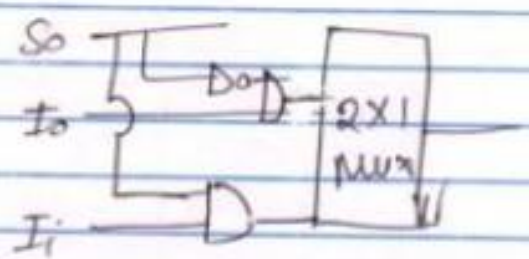


Q. Multiplexer

- A multiplexer is used when multiple data lines are sent to a single channel.
- A multiplexer is a combinational circuit that takes 2^n lines as input & selects one of that line & shows the output.
- A multiplexer is also known as Data selector & it performs the operation of routing using select line. each multiplexer has n select lines.
- A 2×1 Multiplexer.



S_0	I_1
0	I_0
1	I_1



$f = \bar{S}_0 I_0 + S_0 I_1$

4X1 MUX

A 4X1 MUX has 4 input line

$2^2 = 4$

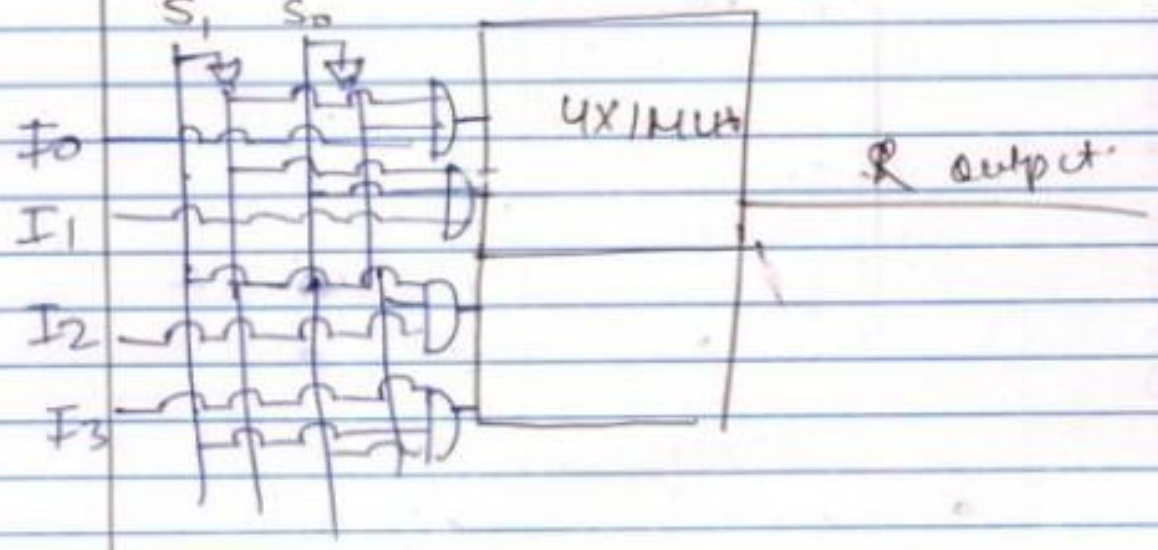
2^n = when n = no. of select line.

∴ it has 2 select lines. S_1, S_0.

and it has 1 output line

S_1	S_0	
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$F = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$



Section-B

Q-2): XOR operator Gate

- XOR is a logicall gate that has 2 inputs & it has one output.
- XOR is a logical which says if both the bits in input are same then the output is false & if both are different then output is true.
- We can also say that if any iput is 0 then output will be 1 & if both inputs are 1 then output is 0.

Truth Table.

A	B	
0	0	0
0	1	1
1	0	1
1	1	0

2. NAND Gate

- Nand is a gate which is the complement of AND gate which means that it gives all the outputs as negation of ~~not~~ AND.

Truth Table.

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

3. NOR Gate

NOR gate is a logical gate that is complement of OR gate which means it shows all output as complement of OR gate.

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

Nand as a universal Gate.

- Nand is considered a universal gate because we can derive all the other logical gates from nand gate only.

example

(OR Gate)

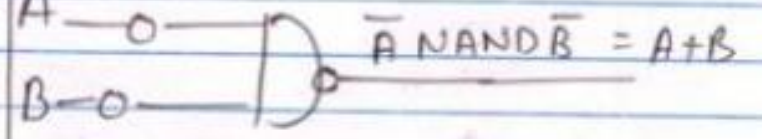
OR gate ⟹

can be implemented using nand gate as -

$((A \cdot B)')' = (\bar{A} + \bar{B})'$

$(\bar{A} + \bar{B})' = A \cdot B$

(NOT A NAND NOT B)

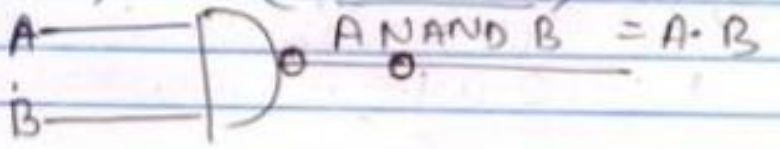


2. AND Gate.

AND ~~op~~ gate $A \cdot B$ 

Can be represented using NAND gates as.

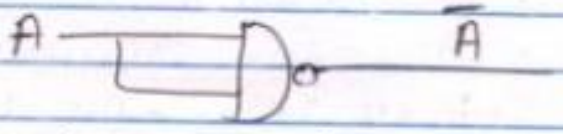
$(\overline{A \cdot B})$ = NOT(A NAND B)



3. NOT Gate

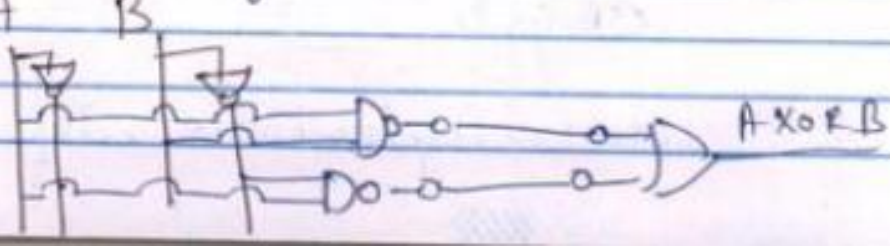
NOT operator gate as $(A)' = \bar{A}$ can be represented as -

A NAND A

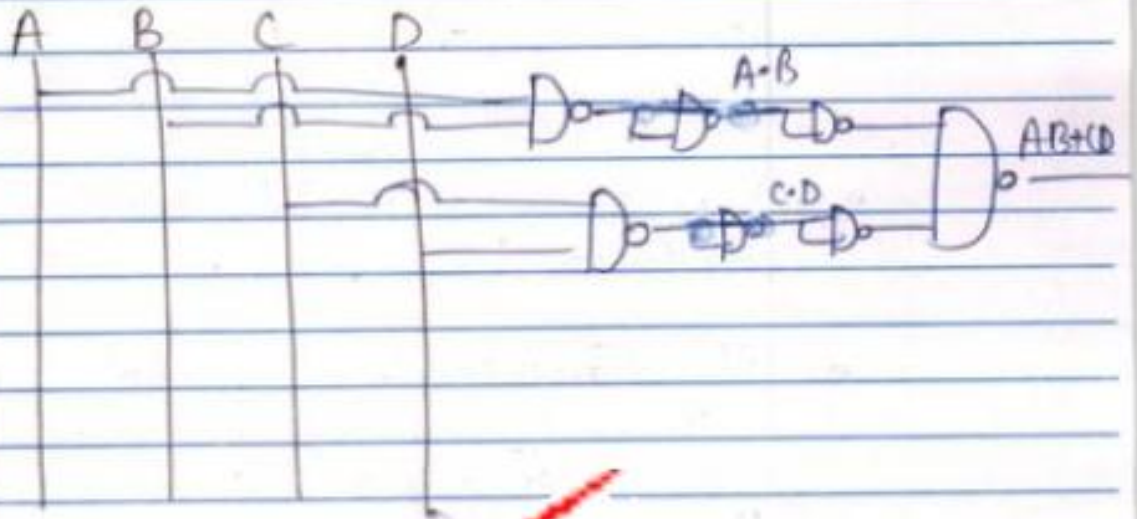


4. XOR gate using

XOR expression is $A'B + B'A$ can be rep using NAND gate as -

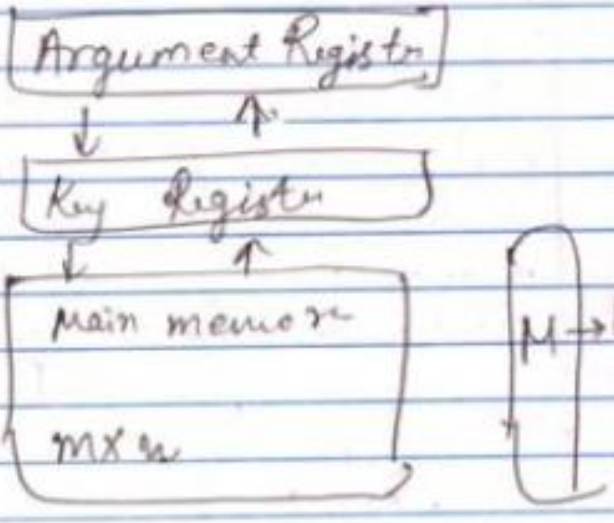


F = AB+CD using NAND Gate



Section-B

9. 1. Associative memory



- An Associative memory is a type of memory which is used to perform searching operation in memory.

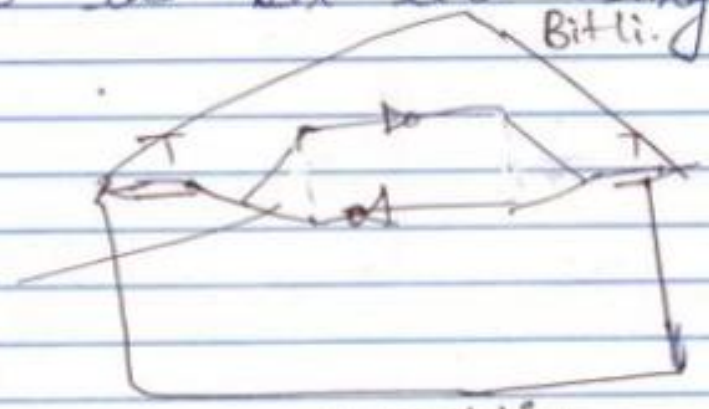
- The searching is done content wise & not ~~data wise~~ address wise so it is also called content addressable memory.
- Here a mxn memory matrix matrix is used with n bits for m data.
- The Argument Register holds the string that is to be searched inside the memory.
  Key Register holds the maps or information about the Argument register
- The Argument Register string is compared sequentially & parallelly to the content of the Main memory & if the match is found then the Match register for that memory string is returned true 1. Otherwise it is returned false 0.

Use of Associative Memory

1. Associative Memory is used to search data from a the memory efficiently with the support of address & only content.

Static RAM

- Its abbreviation is SRAM.
  it is called so because it stores the data statically and does not require any refreshing.
- It uses the latches to retain the data & the latches are connected to the bit line using 2 transistors

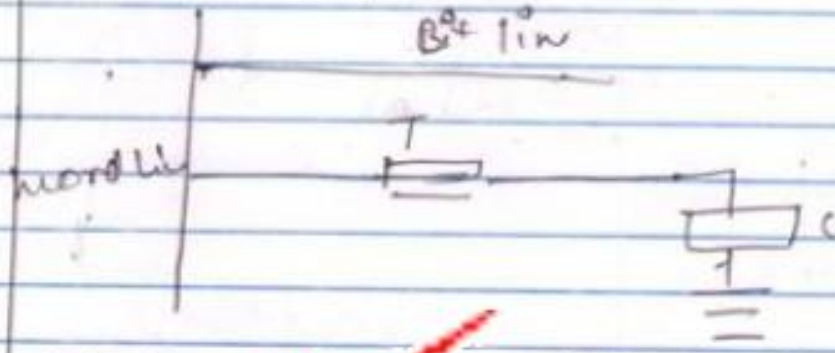


- The data is read & write from the word line.
- Static RAM is a fast & quickly accessable memory. Fast access.
- It is simple to maintain but it is very costly.
- It does not have a high capacity and the memory density is very low.

Use – It is used in the cache memory because it can be accessed very fast & does not need frequent refreshing.

DRAM

- It is a Type of RAM which is formed with the help of capacitors
- It is a non volatile memory because the capacitors used are like a bucket filled with electrons. Here data leaking can happen & to prevent this - They need to be refreshed frequently



- Selected data from Bit line is transfer to word line which is ~~read~~ wh on the capacitors
but capacitors can't keep that data u they are refreshed.
- DRAM is very cheap & it can be easily maintained.
- Its memory capacity is high with high data density.
- It cannot be accessed frequently

Use - The DRAM are used in Main mem because they are volatile and they are to access.