Roll No. .....

Question Booklet Number

O. M. R. Serial No. | | | | | | | | |

M. Sc. (Electronics) (Fourth Semester)

EXAMINATION, July, 2022

(Elective Course)

PROCESSES IN DEVICE FABRICATION

Paper Code				
ELC	4	0	4	(F)

Questions Booklet Series
A

Time : 1:30 Hours] [*Maximum Marks : 100*

Instructions to the Examinee :

1. Do not open the booklet unless you are asked to do so.
2. The booklet contains 60 questions. Examinee is required to answer any 50 questions in the OMR Answer-Sheet provided and not in the question booklet. If more than 50 questions are attempted by student, then the first attempted 50 questions will be considered for evaluation. All questions carry equal marks.
3. Examine the Booklet and the OMR Answer-Sheet very carefully before you proceed. Faulty question booklet due to missing or duplicate pages/questions or having any other discrepancy should be got immediately replaced.

परीक्षार्थियों के लिए निर्देश :

1. प्रश्न-पुस्तिका को तब तक न खोलें जब तक आपसे कहा न जाए।
2. प्रश्न-पुस्तिका में 60 प्रश्न हैं। परीक्षार्थी को किन्हीं 50 प्रश्नों को केवल दी गई OMR आन्सर-शीट पर ही हल करना है, प्रश्न-पुस्तिका पर नहीं। यदि छात्र द्वारा 50 से अधिक प्रश्नों को हल किया जाता है तो प्रारम्भिक हल किये हुए 50 उत्तरों को ही मूल्यांकन हेतु सम्मिलित किया जाएगा। सभी प्रश्नों के अंक समान हैं।
3. प्रश्नों के उत्तर अंकित करने से पूर्व प्रश्न-पुस्तिका तथा OMR आन्सर-शीट को सावधानीपूर्वक देख लें। दोषपूर्ण प्रश्न-पुस्तिका जिसमें कुछ भाग छपने से छूट गए हों या प्रश्न एक से अधिक बार छप गए हों या उसमें किसी अन्य प्रकार की कमी हो, तो उसे तुरन्त बदल लें।

(Remaining instructions on the last page) (शेष निर्देश अन्तिम पृष्ठ पर)

(Only for Rough Work)

1. Which one material is preferred for IC fabrications ?

(A) Silicon

(B) Germanium

(C) Aluminium

(D) Copper

2. The Cz process is used for ..... .

(A) Crystal growth

(B) Metallization

(C) Oxidation

(D) Annealing

3. EGS means ..... .

(A) Electronic Gate Silicon

(B) Electric Gate Silicon

(C) Electronic Grade Silicon

(D) Electric Grade Silicon

4. An IC contains :

(A) Passive elements

(B) Active elements

(C) Both passive and active elements

(D) None of the above

5. The most complicated component fabricated on IC is :

(A) Diode

(B) Resistor

(C) Transistor

(D) Conductor

6. The bottom layer of an IC serves as :

(A) Connector layer

(B) Insulating layer

(C) Substrate layer

(D) None of the above

7. All the active and passive elements are grown on the ..... layer of the IC.

(A) First substrate

(B) The second layer which is a single crystal extension of the substrate

(C) The SiO_2

(D) The polysilicon

8. The second layer of IC is of ..... mils thickness.

(A) 2

(B) 3

(C) 1

(D) 1.5

9. The diffusion of in is done on the ..... .

(A) Substrate laser

(B) Second layer

(C) SiO_2 layer

(D) All of the above

10. Protects the wafer from contamination due to impurities :

(A) SiO_2 layer

(B) Masks

(C) Photoresist layer

(D) Diffusion

11. Selective etching is done using ..... .

(A) Diffusion process

(B) Photolithography process

(C) Metallization process

(D) Masking process

12. Usually, the substrate of IC is made up of ..... .

(A) Germanium metal

(B) Silicon

(C) SiO_2

(D) Aluminium

13. The process of forming an IC on a single silicon chip is known as :

(A) Single process IC

(B) Monolithic IC

(C) Epitaxial IC

(D) All of the above

14. A thin layer of SiO_2 is formed over the epitaxial layer by exposing the wafer to an oxygen atmosphere at a temperature of ..... .

(A) 1500 Degrees C

(B) 2500 Degrees C

(C) 5000 Degrees C

(D) 1000 Degrees C

15. Silicon dioxide helps the penetration of impurities.

(A) True

(B) False

(C) Partially true

(D) All of the above

16. After epitaxial growth the next step for IC fabrication is ..... .

(A) Base diffusion

(B) Emitter diffusion

(C) Metallization

(D) Isolation diffusion

17. The collectors of different transistors are drawn from ..... .

(A) Different isolation regions

(B) Same isolation regions

(C) Epitaxial region

(D) Photoresist region

18. To make *p*-*n* junctions reverse biased, with respect to isolation region the *p*-type substrate must also be held at ..... .

(A) Zero

(B) Unity

(C) Positive potential

(D) Negative potential

19. In base diffusion step ..... impurities are diffused.

(A) *p*-type

(B) *n*-type

(C) Both *p* and *n*-type

(D) None of the above

20. The resistivity of the base layer is ..... the isolation region.

(A) Equal to

(B) Lower than

(C) Higher than

(D) Reciprocal

21. The interconnections are made during ..... .

(A) Emitter diffusion process

(B) Photolithography process

(C) Epitaxial growth

(D) Metallization process

22. For interconnection, aluminium is deposited on the wafer through ..... .

(A) Diffusion

(B) Oxidation

(C) Vacuum deposition

(D) All of the above

23. The ..... technique is used to etch away all the undesired aluminium areas.

(A) Photoresist

(B) Oxidation

(C) Diffusion

(D) Polishing

24. After attaching the chip to a suitable header, the package leads are connected to IC using ..... .

(A) Aluminium wire

(B) Copper wire

(C) Lead wire

(D) All of the above

25. During the photolithographic process the wafer is coated with ..... .

(A) SiO_2

(B) Polysilicon

(C) Photosensitive emulsion

(D) Mask

26. After placing the mask over the photoresist the wafer is subjected to ..... .

(A) UV-rays

(B) Visible light

(C) Infrared rays

(D) All of the above

27. The unexposed portions of the photoresist layer are removed using ..... .

(A) Ethylene

(B) Water

(C) CO_2

(D) Trichloroethylene

28. The integrated circuit is available in ..... size.

(A) Large

(B) Small

(C) Medium

(D) Nano

29. Which of the following components are not fabricated on IC ?

(A) Transistors

(B) Resistors

(C) Diodes

(D) Transformers

30. Which of the following passive components is more difficult to fabricate on integrated circuit ?

(A) FET

(B) Diode

(C) Capacitor

(D) Transistor

31. Which of the following circuits are not made with digital ICs ?

(A) Multiplexers

(B) Demultiplexers

(C) Counters

(D) Shift registers

32. The full form of the SSI is :

(A) Small Scale Industries

(B) Small Scale Integration

(C) Surface Scale Integration

(D) Small Surface Integration

33. When the components size is increased within the IC, then the IC size will be ..... .

(A) Decreased

(B) Increased

(C) No change

(D) IC will damage

34. Which component is not used as an impurity in diffusion process ?

(A) Phosphorus

(B) Boron chloride

(C) Phosphorus pentaoxide

(D) Boron oxide

35. In ion implantation method, penetrating the ions into the silicon wafer depends upon ..... .

(A) Accelerating voltage

(B) Accelerating speed

(C) Accelerating current

(D) All of the above

36. What is the advantage of using ion implantation process ?

(A) Lateral spreading is more

(B) Performed at high temperature

(C) Beam current controlled from outside

(D) Performed at low temperature

37. The major disadvantage of P-N junction isolation technique is :

(A) Formation of Parasitic Resistance

(B) Formation of Parasitic Capacitance

(C) Formation of Isolation Island

(D) None of the above

38. Which isolation technique is used in applications like military and aeroscope ?

(A) Thin film isolation

(B) P-N junction isolation

(C) Barrier isolation

(D) Dielectric isolation

39. Pick out the incorrect statement :

Aluminium is usually used for metallization of most IC as it offers :

(A) Relatively a good conductor

(B) High resistance

(C) Good mechanical bond with silicon

(D) Deposition of aluminium film using vacuum deposition

40. How the aluminium film coating is carried out in metallization process ?

(A) Heating and pouring aluminium in required place.

(B) Aluminium is vacuum evaporated and then condensed.

(C) Placing the aluminium in required place and then heating it using tungsten.

(D) None of the above

41. What type of packing is suitable for Integrated Circuits ?

(A) Metal can package

(B) Dual-in-line package

(C) Ceramic flat package

(D) All of the above

42. Metal can IC packages are available in ..... .

(A) 42 leads

(B) 16 leads

(C) 12 leads

(D) 24 leads

43. What process is used in semiconductor industry to fabricate Integrated Circuits ?

(A) Silicon wafer preparation

(B) Silicon planar process

(C) Epitaxial growth of silicon

(D) Photolithography process

44. What will be the next step after slicing (process) silicon wafers ?

(A) All of the above

(B) Lapping

(C) Polishing

(D) Chemical

45. During ion implantation process (before the ion strike the wafer) the accelerated ions are passed through ..... .

(A) Strong Electric field

(B) Strong Magnetic field

(C) Strong Electric and Magnetic field

(D) None of the above

46. In which method shallow penetration of dopants is possible ?

(A) Ion implantation

(B) Vertical diffusion

(C) Horizontal diffusion

(D) Dopants diffusion

47. Which method is most suitable for silicon crystal growth in silicon wafer preparation ?

(A) Float zone process

(B) Bridgeman-Stockbarger method

(C) Czochralski crystal growth process

(D) Laser heated pedestal growth

48. Which is the most striking feature in monolithic integrated circuit transistor ?

(A) Collector contact is present at the bottom of IC.

(B) Collector contact is present at the top of IC.

(C) Collector contact is absent.

(D) Collector contact is present on one of the sides of IC.

49. Why monolithic IC transistor is preferred over discrete planar epitaxial transistor ?

(A) Due to structural difference

(B) Increase in $V_{CE\ (sat)}$ and collector series resistor

(C) Improvement in circuit performance

(D) All of the above

50. What is the reason for using lateral *p-n-p* transistor is integrated circuits ?

(A) Requires simple process control

(B) Simultaneous fabrication of *p-n-p* and *n-p*-n transistors

(C) Provide good isolation

(D) Miniaturization and cost reduction

51. Which of the following transistor has the limitation, due to the requirement for additional fabrication steps and design consideration ?

(A) Vertical *p-n-p* transistor

(B) Lateral *p-n-p* transistor

(C) Triple diffused *p-n-p* transistor

(D) Substrate *p-n-p* transistor

52. The 'buried layer' reduces collector series resistance by providing ..... .

(A) A low resistivity current path from *n*-type layer to n^+ contact layer

(B) A low resistivity current path from *p*-type layer to n^+ contact layer

(C) A high resistivity current path from *n*-type layer to n^+ contact layer

(D) A high resistivity current path from *p*-type layer to n^+ contact layer

53. At what potential, the substrate of a vertical *p-n-p* transistor should be kept to attain good isolation ?

(A) Same potential

(B) Positive potential

(C) Different potential

(D) Negative potential

54. Which method is used in the fabrication of *p-n-p* transistor ?

(A) Vertical substrate *p-n-p*

(B) Triple diffused *p-n-p*

(C) Lateral *p-n-p*

(D) All of the above

55. The diffusion of collector impurities in *n*-*p*-*n* transistor should be small because ..... .

(A) No additional diffusion or masking steps required

(B) Bandwidth is controlled by lateral diffusion of *p*-type impurity

(C) Collector need not be kept at negative potential

(D) None of the above

56. The advantage of multi-emitter transistor is ..... .

(A) To reduce fabrication steps

(B) To save chip area

(C) To lower design consideration

(D) To provide linear output

57. The number of squares contained in the integrated resistor by diffused resistor method depend on ratio of ..... .

(A) ρ/t

(B) $\rho \times L/W$

(C) $W/L \times t$

(D) L/W

58. Which integrated resistor can achieve high value of sheet resistance ?

(A) Pinched resistor

(B) Epitaxial resistor

(C) Thin film resistor

(D) All of the above

59. Which of the following is not used as metallic film in the thin film resistor ?

(A) Nichrome (NiCr)

(B) Tantalum (Ta)

(C) Stannic oxide (SnO_2)

(D) Silicon dioxide (SiO_2)

60. The capacitance of junction capacitor does not depend upon ..... .

(A) Impurity concentration of *p*-type epitaxial layer

(B) Impurity concentration of *n*-type epitaxial layer

(C) Area of the junction

(D) Voltage across the junction

4. Four alternative answers are mentioned for each question as—A, B, C & D in the booklet. The candidate has to choose the most correct/appropriate answer and mark the same in the OMR Answer-Sheet as per the direction :

Example :

Question :

Q. 1 (A) ● (C) (D)
Q. 2 (A) (B) ● (D)
Q. 3 (A) ● (C) (D)

Illegible answers with cutting and over-writing or half filled circle will be cancelled.

5. Each question carries equal marks. Marks will be awarded according to the number of correct answers you have.

6. All answers are to be given on OMR Answer sheet only. Answers given anywhere other than the place specified in the answer sheet will not be considered valid.

7. Before writing anything on the OMR Answer Sheet, all the instructions given in it should be read carefully.

8. After the completion of the examination candidates should leave the examination hall only after providing their OMR Answer Sheet to the invigilator. Candidate can carry their Question Booklet.

9. There will be no negative marking.

10. Rough work, if any, should be done on the blank pages provided for the purpose in the booklet.

11. To bring and use of log-book, calculator, pager and cellular phone in examination hall is prohibited.

12. In case of any difference found in English and Hindi version of the question, the English version of the question will be held authentic.

Impt. : On opening the question booklet, first check that all the pages of the question booklet are printed properly. If there is ny discrepancy in the question Booklet, then after showing it to the invigilator, get another question Booklet of the same series.

4. प्रश्न-पुस्तिका में प्रत्येक प्रश्न के चार सम्भावित उत्तर— A, B, C एवं D हैं। परीक्षार्थी को उन चारों विकल्पों में से एक सबसे सही अथवा सबसे उपयुक्त उत्तर छाँटना है। उत्तर को OMR आन्सर-शीट में सम्बन्धित प्रश्न संख्या में निम्न प्रकार भरना है :

उदाहरण :

प्रश्न :

प्रश्न 1 (A) ● (C) (D)
प्रश्न 2 (A) (B) ● (D)
प्रश्न 3 (A) ● (C) (D)

अपठनीय उत्तर या ऐसे उत्तर जिन्हें काटा या बदला गया है, या गोले में आधा भरकर दिया गया, उन्हें निरस्त कर दिया जाएगा।

5. प्रत्येक प्रश्न के अंक समान हैं। आपके जितने उत्तर सही होंगे, उन्हीं के अनुसार अंक प्रदान किये जायेंगे।

6. सभी उत्तर केवल ओ. एम. आर. उत्तर-पत्रक (OMR Answer Sheet) पर ही दिये जाने हैं। उत्तर-पत्रक में निर्धारित स्थान के अलावा अन्यत्र कहीं पर दिया गया उत्तर मान्य नहीं होगा।

7. ओ. एम. आर. उत्तर-पत्रक (OMR Answer Sheet) पर कुछ भी लिखने से पूर्व उसमें दिये गये सभी अनुदेशों को सावधानीपूर्वक पढ़ लिया जाये।

8. परीक्षा समाप्ति के उपरान्त परीक्षार्थी कक्ष निरीक्षक को अपनी OMR Answer Sheet उपलब्ध कराने के बाद ही परीक्षा कक्ष से प्रस्थान करें। परीक्षार्थी अपने साथ प्रश्न-पुस्तिका ले जा सकते हैं।

9. निगेटिव मार्किंग नहीं है।

10. कोई भी रफ कार्य, प्रश्न-पुस्तिका के अन्त में, रफ-कार्य के लिए दिए खाली पेज पर ही किया जाना चाहिए।

11. परीक्षा-कक्ष में लॉग-बुक, कैलकुलेटर, पेजर तथा सेल्युलर फोन ले जाना तथा उसका उपयोग करना वर्जित है।

12. प्रश्न के हिन्दी एवं अंग्रेजी रूपान्तरण में भिन्नता होने की दशा में प्रश्न का अंग्रेजी रूपान्तरण ही मान्य होगा।

महत्वपूर्ण : प्रश्नपुस्तिका खोलने पर प्रथमतः जाँच कर देख लें कि प्रश्न-पुस्तिका के सभी पृष्ठ भलीभाँति छपे हुए हैं। यदि प्रश्नपुस्तिका में कोई कमी हो, तो कक्षनिरीक्षक को दिखाकर उसी सिरीज की दूसरी प्रश्न-पुस्तिका प्राप्त कर लें।