Roll No	•••••					Question Booklet Number
O. M. R. Serial No.						

M. Sc. (Electronics) (Second Semester) (NEP) EXAMINATION, 2022-23

DIGITAL SYSTEM AND DESIGN

Paper Code							
В	1	4	0	8	0	4	T

Time : 1:30 Hours]

Questions Booklet Series

A

[Maximum Marks : 75

Instructions to the Examinee:

- 1. Do not open the booklet unless you are asked to do so.
- The booklet contains 100 questions.
 Examinee is required to answer 75 questions in the OMR Answer-Sheet provided and not in the question booklet.
 All questions carry equal marks.
- 3. Examine the Booklet and the OMR Answer-Sheet very carefully before you proceed. Faulty question booklet due to missing or duplicate pages/questions or having any other discrepancy should be got immediately replaced.

परीक्षार्थियों के लिए निर्देश :

- प्रश्न-पुस्तिका को तब तक न खोलें जब तक आपसे कहा न जाए।
- 2. प्रश्न-पुस्तिका में 100 प्रश्न हैं। परीक्षार्थी को 75 प्रश्नों को केवल दी गई OMR आन्सर-शीट पर ही हल करना है, प्रश्न-पुस्तिका पर नहीं। सभी प्रश्नों के अंक समान हैं।
- 3. प्रश्नों के उत्तर अंकित करने से पूर्व प्रश्न-पुस्तिका तथा

 OMR आन्सर-शीट को सावधानीपूर्वक देख लें। दोषपूर्ण

 प्रश्न-पुस्तिका जिसमें कुछ भाग छपने से छूट गए हों या

 प्रश्न एक से अधिक बार छप गए हों या उसमें किसी

 अन्य प्रकार की कमी हो, तो उसे तुरन्त बदल लें।

(शेष निर्देश अन्तिम पृष्ठ पर)

(Remaining instructions on the last page)

(Only for Rough Work)

B140	804T (3)	Set-A
	(D) Digital counter		(D) 65, 536 locations
	(C) Decoder		(C) 256 locations
	(B) Demultiplexer		(B) 16 locations
	(A) Multiplexer		(A) 8 locations
	used as parallel to serial converter?		·
4.	Which of the following circuit can be	0.	code can select in memory ?
	Semiconductor	8.	How much locations an 4-bit address
	(D) Complementary Metal Oxide		(D) When the inputs are all one
	Semiconductor		(C) When the inputs are all zero
	(C) Continuous Metal Oxide		•
	Semiconductor		(B) When the clock is positive
	(B) Concrete Metal Oxide		(A) When the clock is negative
	Semiconductor Semiconductor		state ?
<i>J</i> .	(A) Centred Metal Oxide		flop in Digital Electronics changes its
3.	CMOS refers to	7.	When does a positive level triggered flip-
	(D) NAND		
	(C) SOP		(D) $J'K' + KQn$
	(A) AND (B) POS		(C) $J' + KQn$
	operation. (A) AND		(B) $JQn' + K'Qn$
	(X + Z) shows the		(A) $J + K'Qn$
2.	The expression $Y = (X + Y)(Y + Z)$		flop is
	(D) 12 bits	6.	The characteristics equation of J-K flip-
	(C) 8 bits		(D) None of the above
	(B) 4 bits		(D) None of the above
	(A) 2 bits		(C) Time delay switch
	conventional BCD format.		(B) Toggle switch
	for representation in the		(A) Transfer data circuit
1.	A two digit decimal number requires	5.	T flip-flop is used as

	PLD?		(A) 64 bits
	(A) To protect from high voltage		(B) 32 bits
	(B) To increase the memory		(C) 16 bits
	(C) To implement the programmes		(D) 8 bits
	(D) As a switching devices		(D) outs
10.	The minimum number of flip-flops that	14.	Perform binary addition: 110011 +
	can be used to construct a modulus-7		101010 = ?
	counter is		(A) 011010
	(A) 3		(B) 1010100
	(B) 7		(C) 100110
	(C) 8		(D) 1011101
	(D) 10		
11.	The parameter through which 8 distinct	15.	The given hexadecimal number (2F.67) ₁₆
	values can be represented is known as		is equivalent to
			(A) (57.316) ₈
	(A) Bit		(B) (55.246) ₈
	(B) Byte		(C) (57.340) ₈
	(C) Word		(D) (55.599) ₈
	(D) Nibble		(-) ()
12.	The largest four digit hexadecimal	16.	The total storage capacity of 2K * 8
	number is		ROM is
	(A) (FFEE) 16		(A) 8 bits
	(B) (FFDD)16		(B) 16 bits
	(C) (FFFF)16		(C) 1024 bits
	(D) (EEFF)16		(D) 2048 bits

Why antifuses are implemented in a 13. The quantity of quad word is

9.

	(10.1	(0), we get		by us	ing
	(A)	101.0010		(A)	Adder
	(B)	0010.101		(B)	Comparator
	(C)	011.0010		(C)	Inverter
	(D)	110.0011		(D)	Subtractor
18.	2's	complement of 10101010 is	22	. The	decimal equivalent of the binary
	•••••			numb	per (1110.011)2 is
	(A)	01010110		(A)	(11.175)10
	(B)	11010100		(B)	(14.375)10
	(C)	11100010		(C)	(12.175)10
	(D)	00110101		(D)	(14.275)10
19.	Perfo	orm binary subtraction : 111011 –	23	. There	e are Minterms for 4
	1011	10 = ?		varial	bles (a, b, c, d) .
	(A)	100100		(A)	4
	(B)	010101		(B)	8
	(C)	001101		(C)	16
		011001		(D)	32
20.	Repr	resentation of hexadecimal number	24	. How	many two-input AND and OR gates
	-	C)H in decimal :		are re	quired to realize $Y = AB + CD + E$?
	(A)	$15 * 16^2 + 6 * 16^1 + 12 * 16^0$		(A)	2, 2
	(B)	$12 * 16^2 + 6 * 16^1 + 15 * 16^0$		(B)	3, 2
	(C)	$14 * 16^2 + 6 * 16^1 + 12 * 16^0$		(C)	3, 3
	(D)	$15 * 16^2 + 6 * 16^1 + 14 * 16^0$		(D)	2, 3
B140	804T	(5)		Set-A

17. On binary multiplication of (01.01) and 21. 1's complement can be easily obtained

A 3-bit counter has a maximum modulus	29.	What will be the output from a D flip-
of		flop if $D = 1$ and the clock is low?
(A) 3		(A) 1
(B) 6		(B) 0
(C) 8		(C) No change
(D) 16		(D) Toggle between 0 and 1
A flip-flop stores	30.	In a J-K flip-flop, if J = K the resulting
(A) 2 bit of information		flip-flop is referred to as
(B) 4 bit of information		(A) T flip-flop
(C) 1 bit of information		(B) S-K flip-flop
(D) 3-bit information		(C) D flip-flop
Which of the following best describes		(D) S-R flip-flop
EEPROMs?	31.	Exclusive-NOR (Ex-NOR) logic gates
(A) EEPROMs can be programmed		can be constructed from what other logic
only once		gates ?
(B) EEPROMs can be erased by UV		(A) OR gates only
(C) EEPROMs can be erased by		(B) OR gates and NOT gates
shorting all inputs to the ground		(C) AND gates and NOT gates
(D) EEPROMs can be erased		(D) AND gates, OR gates, and NOT
electrically		gates
Ripple counters are	32.	The logical product of two or more
(A) Synchronous counters		logical sum terms is called
(B) Asynchronous counters		(A) SOP
(B) Asynchronous counters(C) True binary counters		(A) SOP(B) POS
•		· •
	 (A) 3 (B) 6 (C) 8 (D) 16 A flip-flop stores	 (A) 3 (B) 6 (C) 8 (D) 16 A flip-flop stores

33.	There are cells in a 3-variable	38.	Which A/D converter is considered to be		
	K-map.		simplest, fastest and most expensive?		
	(A) 12		(A) Flash type ADC		
	(B) 16		(A) Plasti type ADC		
	(C) 6		(B) Servo converter		
	(D) 8		(C) Counter type ADC		
34.	A full subtractor logic circuit will have		(D) All of the mentioned		
	(A) Three inputs and two outputs	39.	PLA contains		
	(B) Three inputs and three outputs		(A) NOR and OR arrays		
	(C) Two inputs and two outputs		(B) NOT and OR arrays		
	(D) Two inputs and one output		•		
35.	DeMorgan's theorem states that		(C) NAND and NOT arrays		
			(D) AND and OR arrays		
	(A) $(A + B)' = A' * B'$	40.	The given havedesimal number (F0), is		
	(B) $(A + B)' = A' * B$	40.	The given hexadecimal number $(E9)_{16}$ is		
	(C) A' + B' = A'B'		equivalent to Gray Code.		
	(D) $(AB)' = A' + B$		(A) 10011101		
36.	AT flip-flop can be constructed from a		(B) 11001001		
	flip-flop.				
	(A) S-R		(C) 10101010		
	(B) J-K		(D) 11011111		
	(C) D	41	DAMe are willed in the common		
	(D) S-K	41.	RAMs are utilized in the computer		
37.	The terminal count of a typical modulus-		as		
	12 binary counter is		(A) Scratch-pad		
	(A) 0000		(B) Main memory		
	(B) 1010		(C) Buffer		
	(C) 1011				
	(D) 1111		(D) All of the Mentioned		

42.	Drawback of counter type A/D converter:	46.	A minimum of parity
	(A) Counter reset automatically		bits are required for generating Hamming
	(B) Low speed		code for 8421 code.
	(C) High conversion time		(A) 2
	(D) More complex		(B) 3
	(=)		(C) 4
43.	The full form of EPROM is		(D) 5
	(A) Electrically Programmable ROMs	47.	Gray code is a
	(B) Erasable Programming ROMS		(A) Standard
	(C) Erasable Programmable ROMs		(B) Universal
	(D) Erasable Programmed ROMs		(C) Weighted
			(D) Non-weighted
44.	The radix of a octal number system	48.	Schottky TTL has
	is		propogation delay time than TTL.
	(A) 2		(A) Lower
	(B) 8		(B) Higher
	(C) 10		(C) Zero
	(D) 16		(D) None of the above
45.	If A and B are the inputs of a half adder,	49.	In a J-K flip flop if $J = K = 1$, its Q
	the carry is given by		output will be when a
	, c		clock pluse is applied.
	(A) A AND B		(A) Reset
	(B) A OR B		(B) Set
	(C) A XOR B		(C) Compliment
	(D) A EX-NOR B		(D) Unchange
	(D) A EX-NOR B		(D) Unchange

50.	The design of an ALU is based	53.	Fan-in and Fan-out are the characteristics
	on		of
	(A) Sequential logic		(A) Counters
	(B) De-Multiplexing		(B) Combinational Circuits
	(C) Multiplexing		(C) Sequential Circuits
	(D) Combinational logic		(D) Logic families
5 1	The output of a full odder is some as	54.	All logic operations can be obtained by
51.	The output of a full adder is same as		means of
			(A) NAND and NOR operations
	(A) Decoder		(B) AND and OR operations
	(B) Full subtractor		(C) OR and NOT operations
	(C) Half subtractor		(D) AND and NOT operations
	(D) Half adder	55.	The number of bits required to represent
52.	The following switching functions are to		25 in BCD is
	be implemented using a decoder:		(A) 4
	$f1 = \sum m(1, 3, 4, 8, 10)$ and		(B) 8
	$f2 = \Sigma \ m(2, 4, 5, 9, 11, 14)$		(C) 12
			(D) 16
	The minimum configuration of decoder	56.	Master-slave configuration is used in a
	will be		J-K flip-flop to eliminate
	(A) 2 to 4 line		(A) Race around condition
	(B) 3 to 8 line		(B) Set condition
	(C) 4 to 16 line		(C) Reset condition
	(D) 5 to 32 line		(D) Compliment condition

57.	Registers can be designed using	61.	DRAM stores single bit by using
	(A) Counter		(A) Transistor
	(B) Decoder		(B) Capacitor
	(C) Flip-flop		(C) Both (A) and (B)
	(D) Encoder		(D) None of the above
58.	The speed of an asynchronous counter is than that of a synchronous	62.	The components used in DTL logic
	counter.		are
	(A) Less		(A) Diode, transistor
	(B) Greater		(B) Diode, resistor
	(C) Equal		(C) Diode, transistor, resistor
	(D) None of the above		(D) None of the above
59.	A dynamic RAM is fabricated usingtechnology.	63.	The group of flip-flops is also known
	(A) TTL		as
	(B) MOS		(A) Registers
	(C) DTL		(B) Decoders
	(D) None of the above		(C) Encoders
60.	If A, B and C are the inputs of a full		(D) None of the above
	adder then the carry is given by	64.	The output of the multiplexer depends on
	(A) A AND B OR (A OR B) AND C		its
	(B) A OR B OR (A AND B) C		(A) Data outputs
	(C) (A AND B) OR (A AND B)C		(B) Data inputs
	(D) A XOR B XOR (A XOR B)		(C) Selected inputs
	AND C		(D) None of the above

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	(D)	None of the above		(D)	None of the above
	, ,			(C)	NOT gate
	(C)	$2^{P} \ge P - m - 1$		(B)	OR gate
	(B)	$2^{P} \ge P + m - 1$		(A)	AND gate
	(A)	$2^{P} \ge P + m + 1$			ected together. The resulting circuit
	of pa	rity bits ?	71.		inputs of a NAND gate are
67.	Wha	t is the formula to obtain the number		(D)	J = 1, K = 0
	(D)	None of the above		(C)	J = 0, K = 0
	(C)	Three terminal device		(B)	J = 1, K = 1
	(C)	Three terminal devices		(A)	J = 0, K = 1
	(B)	Double terminal device	70.	In th	e toggle mode, a JK flip-flop has :
	(A)	Single terminal device		(D)	All of the above
		device.		(C)	NMOS
66.	The	Field Effect Transistor is		(B)	CMOS
66	The	Field Effect Transistor is		(A)	PMOS
	(D)	None of the above	UZ.	fami	
	(C)	Present state	69.	` ′	comes under unipolar logic
	(B)	Present input and present state		(C) (D)	Pulses None of the above
	(A)	Present input		(B)	Bits
	((A)	Digits
	depends on			of	

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65. The output of the sequential circuit 68. The counter is used to count the number

72.	Stora	ge of 1 KB means the following	75.	The p	parity is used to
	numb	per of bytes :		(A)	Increase the switching operation
	(A)	1064		(B)	Reduce switching operation
	, ,			(C)	Detect errors
	(B)	1024		(D)	None of the above
	(C)	1000	76.	Whic	ch of the following is an invalid state
	(D)	924		in an	8421 binary coded decimal ?
73.	The t	ime required for a gate to change its		(A)	1001
73.	The time required for a gate to change its			(B)	1101
	outpu	output is called as:		(C)	1000
	(A)	decay time		(D)	0100
	(B)	run time	77.	A th	nree input NOR gate gives high
	(C)	propagation time		outpu	ut when
	(D)	start time		(A)	One input is high
74	How	many input and output required for		(B)	One input is low
74.	пом	many input and output required for		(C)	All inputs are low
	demu	ıltiplexer ?		(D)	All inputs are high
	(A)	one input and many output	78.	A dec	cade counter requires
	(B)	one input and one output		(A)	4 flip-flop
	(C)	number of selection inputs and one		(B)	10 flip-flop
		output		(C)	2 flip-flop
	(D)	None of the answers		(D)	3 flip-flop

(12)

Set-A

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79.	The binary equivalent of decimal number	83.	Excess-3 code is known as
	56 is		(A) Weighted code
	(A) 101101		(B) Cyclic redundancy code
	(B) 110110		(C) Self-complementing code
	(C) 101010		(D) Algebraic code
	(D) 111000		
80.	Group of 4-bits forms	84.	The NOR gate is OR gate followed by
	(A) Nibble		(A) NOT gate
	(B) Byte		(B) NAND gate
	(C) Gigabyte		- · ·
	(D) Terabyte		(C) AND gate
81.	What is the octal equivalent of the binary		(D) None of the above
	number 10111101 ?	85.	How many NAND gates are used to form
	(A) 675		an AND gate ?
	(B) 275		(A) 1
	(C) 572		(B) 2
	(D) 465		(C) 3
82.	An OR gate has 6 inputs. The number of		(D) 4
	input words in its truth table	86.	As the number of inputs increases, the
	are		NAND gate delay:
	(A) 6		(A) increases
	(B) 32		(B) decreases
	(C) 64		(C) does not vary
			(-)

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	(D) (598) ₈		(D) $a = b$
	(C) (640) ₈		(C) $a < b$
	(B) (619) ₈		(B) $a-b$
	(A) $(641)_8$		(A) $a > b$
	number (4174) ₁₀ is		Comparator:
90.	The octal equivalent of the deci	94. mal	One that is not the outcome of Magnitude
	(D) Inductance and capacitance		(D) None of the above
	(C) Transistor		(C) SOP
	(B) Resistance and capacitance		(B) Literals
	(A) Two diodes		(A) POS
07.	using	peu	circuits.
89.	An inverter gates can be develo	med	implemented using 2-level NAND logic
	(D) 2	93.	expressions can be
	(C) 3		(D) AB'
	(B) 4		(C) AB
	(A) 5		(B) 0
	XOR gate ?	iput	(A) 1
88.	What is the minimum number of 2 in NAND gate required to make a 2 in	· ,2.	$(A+B)(A'\cdot B')=?$
00			(D) 00010010
	(C) 2 input XOR gate(D) 2 input XNOR gate		(C) 00111011
	(B) 2 input AND gate		(B) 10101010
	(A) 2 input NAND gate		(A) 11001100
	detector?		compliment we get :

87. Which gate is called as inequality 91. On addition of +38 and -20 using 2's

95.	A combinational circuit that select one	98.	Which one of the following is volatile in
	from many inputs are		nature ?
	(A) Encoder		(A) ROM
	(B) Decoder		(B) EPROM
	(C) De-multiplexer		(C) PROM
	(D) Multiplexer		(D) RAM
96.	How many outputs will a decimal to	99.	A shift register in which the output of the
	BCD encoder have ?		last flip-flop is connected to the Input of
			the first flip-flop?
	(A) 4		(A) P'
	(B) 8		(A) Ring counter
	(C) 12		(B) BCD counter
	(D) 16		(C) Parallel counter
97.	What is the difference between a		(D) Ripple counter
<i>)</i>		100	Which of the following is not a
	shift-right register and a shift-left	100.	-
	register?		decoder?
	(A) There is no difference		(A) 4 to 2
	(B) The direction of the shift		(B) 3 to 8
	(C) Propagation delay		(C) 4 to 16
	(D) The clock input		(D) 5 to 32

(15)

Set-A

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4. Four alternative answers are mentioned for each question as—A, B, C & D in the booklet. The candidate has to choose the correct answer and mark the same in the OMR Answer-Sheet as per the direction:

Example:

Question:

Q. 1 (A) (C) (D) (Q. 2 (A) (B) (D) (D)

Q.3 A \bigcirc C D

Illegible answers with cutting and over-writing or half filled circle will be cancelled.

- 5. Each question carries equal marks. Marks will be awarded according to the number of correct answers you have.
- 6. All answers are to be given on OMR Answer sheet only. Answers given anywhere other than the place specified in the answer sheet will not be considered valid.
- 7. Before writing anything on the OMR Answer Sheet, all the instructions given in it should be read carefully.
- 8. After the completion of the examination candidates should leave the examination hall only after providing their OMR Answer Sheet to the invigilator. Candidate can carry their Question Booklet.
- 9. There will be no negative marking.
- 10. Rough work, if any, should be done on the blank pages provided for the purpose in the booklet.
- 11. To bring and use of log-book, calculator, pager and cellular phone in examination hall is prohibited.
- 12. In case of any difference found in English and Hindi version of the question, the English version of the question will be held authentic.
- Impt.: On opening the question booklet, first check that all the pages of the question booklet are printed properly. If there is ny discrepancy in the question Booklet, then after showing it to the invigilator, get another question Booklet of the same series.

4. प्रश्न-पुस्तिका में प्रत्येक प्रश्न के चार सम्भावित उत्तर—
A, B, C एवं D हैं। परीक्षार्थी को उन चारों विकल्पों में से
सही उत्तर छाँटना है। उत्तर को OMR आन्सर-शीट में
सम्बन्धित प्रश्न संख्या में निम्न प्रकार भरना है:

उदाहरण :

प्रश्न :

 प्रश्न 1 (A)
 (C)
 (D)

 प्रश्न 2 (A)
 (B)
 (D)

 (A)
 (D)

अपठनीय उत्तर या ऐसे उत्तर जिन्हें काटा या बदला गया है, या गोले में आधा भरकर दिया गया, उन्हें निरस्त कर दिया जाएगा।

- 5. प्रत्येक प्रश्न के अंक समान हैं। आपके जितने उत्तर सही होंगे, उन्हीं के अनुसार अंक प्रदान किये जायेंगे।
- 6. सभी उत्तर केवल ओ. एम. आर. उत्तर-पत्रक (OMR Answer Sheet) पर ही दिये जाने हैं। उत्तर-पत्रक में निर्धारित स्थान के अलावा अन्यत्र कहीं पर दिया गया उत्तर मान्य नहीं होगा।
- 7. ओ. एम. आर. उत्तर-पत्रक (OMR Answer Sheet) पर कुछ भी लिखने से पूर्व उसमें दिये गये सभी अनुदेशों को सावधानीपूर्वक पढ लिया जाये।
- 8. परीक्षा समाप्ति के उपरान्त परीक्षार्थी कक्ष निरीक्षक को अपनी OMR Answer Sheet उपलब्ध कराने के बाद ही परीक्षा कक्ष से प्रस्थान करें। परीक्षार्थी अपने साथ प्रश्न-पुस्तिका ले जा सकते हैं।
- 9. निगेटिव मार्किंग नहीं है।
- 10. कोई भी रफ कार्य, प्रश्न-पुस्तिका के अन्त में, रफ-कार्य के लिए दिए खाली पेज पर ही किया जाना चाहिए।
- 11. परीक्षा-कक्ष में लॉग-बुक, कैलकुलेटर, पेजर तथा सेल्युलर फोन ले जाना तथा उसका उपयोग करना वर्जित है।
- 12. प्रश्न के हिन्दी एवं अंग्रेजी रूपान्तरण में भिन्नता होने की दशा में प्रश्न का अंग्रेजी रूपान्तरण ही मान्य होगा।

महत्वपूर्ण : प्रश्नपुस्तिका खोलने पर प्रथमतः जाँच कर देख लें कि प्रश्न-पुस्तिका के सभी पृष्ठ भलीभाँति छपे हुए हैं। यदि प्रश्नपुस्तिका में कोई कमी हो, तो कक्षनिरीक्षक को दिखाकर उसी सिरीज की दूसरी प्रश्न-पुस्तिका प्राप्त कर लें।