Roll No. ....

O. M. R. Serial No.

B. C. A. (Second Semester) (B. P.)

EXAMINATION, 2022-23

DIGITAL ELECTRONICS & COMPUTER ORGANIZATION

Paper Code
B C A 2 0 2 N

Time : 1:30 Hours]

[*Maximum Marks : 75*

Instructions to the Examinee :

1. Do not open the booklet unless you are asked to do so.

2. The booklet contains 100 questions. Examinee is required to answer 75 questions in the OMR Answer-Sheet provided and not in the question booklet. All questions carry equal marks.

3. Examine the Booklet and the OMR Answer-Sheet very carefully before you proceed. Faulty question booklet due to missing or duplicate pages/questions or having any other discrepancy should be got immediately replaced.

परीक्षार्थियों के लिए निर्देश :

1. प्रश्न-पुस्तिका को तब तक न खोलें जब तक आपसे कहा न जाए।

2. प्रश्न-पुस्तिका में 100 प्रश्न हैं। परीक्षार्थी को 75 प्रश्नों को केवल दी गई OMR आन्सर-शीट पर ही हल करना है, प्रश्न-पुस्तिका पर नहीं। सभी प्रश्नों के अंक समान हैं।

3. प्रश्नों के उत्तर अंकित करने से पूर्व प्रश्न-पुस्तिका तथा OMR आन्सर-शीट को सावधानीपूर्वक देख लें। दोषपूर्ण प्रश्न-पुस्तिका जिसमें कुछ भाग छपने से छूट गए हों या प्रश्न एक से अधिक बार छप गए हों या उसमें किसी अन्य प्रकार की कमी हो, तो उसे तुरन्त बदल लें।

(Remaining instructions on the last page)

(शेष निर्देश अन्तिम पृष्ठ पर)

(Only for Rough Work)

1. A + AB + ABC + ABCD + ABCDE
   + ... =
   (A) 1
   (B) A
   (C) A + AB
   (D) AB

2. The simplified form of the Boolean expression (X + Y + XY)(X + Z) is :
   (A) X + Y + Z
   (B) XY + YZ
   (C) X + YZ
   (D) XZ + Y

3. BCD is :
   (A) Binary Coded Decimal
   (B) Bit Coded Decimal
   (C) Binary Coded Digit
   (D) Bit Coded Digit

4. A + B = B + A; AB = BA represent which law ?
   (A) Commutative
   (B) Associative
   (C) Distributive
   (D) Idempotence

5. The logic expression $AB + \bar{B}C + AC$ is in :
   (A) SOP form
   (B) POS form
   (C) standard SOP form
   (D) standard POS form

6. The number of cells in a 6- variable K-map is :
   (A) 6
   (B) 12
   (C) 36
   (D) 64

7. The code used for labelling cells of the K-map is :
   (A) natural BCD
   (B) Hexadecimal
   (C) Gray
   (D) Octal

8. Which of the following methods is used to minimize Boolean expressions ?
   (A) Fourier transform
   (B) Gray code
   (C) Karnaugh mapping
   (D) Venitch method

9. Four adjacent '1's in a Karnaugh map forms a/an :

(A) octet

(B) singlet

(C) pair

(D) quad

10. Don't care conditions can be used for simplifying Boolean expression in :

(A) Logic diagram

(B) Minterms

(C) K-maps

(D) Maxterms

11. In a Karnaugh map the formation of Quad results in the elimination of .... variables and their complements.

(A) 2

(B) 3

(C) 4

(D) 8

12. A 2-level AND-OR logic circuit is used to express :

(A) Product of sum

(B) Sum of product

(C) Boolean expression

(D) All of the above

13. Product-of-Sums expressions can be implemented using :

(A) 2-level OR-AND logic circuits

(B) 2-level NOR logic circuits

(C) Both (A) and (B)

(D) None of the above

14. The output is dependent on present output :

(A) Combinational Circuit

(B) Analog circuit

(C) Flip Flop

(D) Sequential Circuit

15. In an SR latch built from NOR gates, which condition is not allowed ?

(A) S = 0, R = 0

(B) S = 0, R = 1

(C) S = 1, R = 0

(D) S = 1, R = 1

16. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder ?

(A) 1

(B) 2

(C) 4

(D) 8

17. Convert BCD 0001 0010 0110 to binary.

    (A) 1111110

    (B) 1111101

    (C) 1111000

    (D) 1111111

18. The number of full and half adders required to add 16-bit number is :

    (A) 8 half adders, 8 full adders

    (B) 1 half adders, 15 full adders

    (C) 16 half adders, 0 full adders

    (D) 4 half adders, 12 full adders

19. How many data select lines are required for selecting 8 inputs ?

    (A) 1

    (B) 2

    (C) 3

    (D) 4

20. How many possible outputs would a decoder have with a 6-bit number ?

    (A) 16

    (B) 32

    (C) 64

    (D) 128

21. A combinational circuit :

    (A) always contains memory elements

    (B) never contains memory elements

    (C) may sometimes contain memory elements

    (D) contains only memory elements

22. .... are an example of a combinational circuit.

    (A) Shift registers

    (B) Multiplexers

    (C) Counters

    (D) Flip-flops

23. In the toggle mode, a JT flip-flop has :

    (A) J = 0, K = 1

    (B) J = 1, K = 1

    (C) J = 0, K = 0

    (D) J = 1, K = 0

24. A digital circuit that can store only one bit is a :

    (A) Register

    (B) NOR gate

    (C) Flip-flop

    (D) XOR gate

25. DeMorgan's Law states that :

(A) (A + B)' = A' * B

(B) (AB)' = A' + B'

(C) (AB)' = A' + B

(D) (AB)' = A + B

26. Suppose that the output of an XNOR gate is 1. Which of the given input combinations is correct ?

(A) A = 0, B' = 1

(B) A = 1, B = 1

(C) A = 0, B = 1

(D) A = 0, B = 0

27. Number of 2 input multiplexers need to construct a 2^{10} inputs multiplexer is :

(A) 32

(B) 9

(C) 129

(D) 1023

28. The main equation for a D flip-flop is :

(A) Q = 0

(B) Q = 1

(C) Q = D

(D) Q = D'

29. A flip-flop is a .... circuit.

(A) Combinational

(B) Sequential

(C) Both (A) and (B)

(D) None of the above

30. Which GATE is called INEQUALITY COMPARATOR ?

(A) NOR

(B) NOT

(C) AND

(D) XOR

31. How many flip-flops are required to build a binary counter circuit to count from 0 to 1023 ?

(A) 6

(B) 10

(C) 24

(D) 12

32. In flip-flop clock is present but in latch clock is :

(A) present always

(B) absent always

(C) may be present/absent

(D) None of the above

33. Each term in the standard SOP form is called a :

(A) minterm

(B) maxterm

(C) literal

(D) don't care

34. Which one of the following is known as a data distributor ?

(A) Demultiplexer

(B) Decoder

(C) Multiplexer

(D) All of the above

35. Which one of the following is an operating principle for demultiplexer ?

(A) One to many

(B) Many to one

(C) Both (A) and (B)

(D) None of the above

36. In which one of the following logic circuits the feedback loop is not present ?

(A) Sequential logic circuit

(B) Combinational logic circuit

(C) Both (A) and (B)

(D) None of the above

37. Whenever the data is found in the cache memory it is called as ....

(A) HIT

(B) MISS

(C) FOUND

(D) ERROR

38. The Boot sector files of the system are stored in which computer memory ?

(A) RAM

(B) ROM

(C) Cache

(D) Register

39. Which of the following is the lowest in the computer memory hierarchy ?

(A) Cache

(B) RAM

(C) Secondary memory

(D) CPU registers

40. Which memory acts as a buffer between CPU and main memory ?

(A) RAM

(B) ROM

(C) Cache

(D) Storage

41. Which process is used to map logical addresses of variable length onto physical memory ?

(A) Paging

(B) Overlays

(C) Segmentation

(D) Paging with segmentation

42. The transformation of data from main memory to cache memory is referred to as a/an ....

(A) transfer rate

(B) access time

(C) mapping process

(D) None of above

43. In direct mapping cache organization, the CPU address is divided into which two fields ?

(A) Index, Code

(B) Sequence,Tag

(C) Index, Tag

(D) None of the above

44. The main memory is 4K × 9 and cache memory is 512 × 9 in direct mapping. Index field of cache memory is ....

(A) 9 bits

(B) 6 bits

(C) 3 bits

(D) 12 bits

45. The main memory is 4K × 9 and cache memory is 512 × 9 in direct mapping. Tag field of cache memory is ....

(A) 9 bits

(B) 6 bits

(C) 3 bits

(D) l2 bits

46. On the fifth clock pulse, a 4-bit Johnson sequence is $Q_0 = 0$, $Q_1 = 1$, $Q_2 = 1$, and $Q_3 = 1$. On the sixth clock pulse, the sequence is ....

(A) $Q_0 = 1$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$

(B) $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 1$, $Q_3 = 0$

(C) $Q_0 = 0$, $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 1$

(D) $Q_0 = 0$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 1$

47. How can parallel data be taken out of a shift register simultaneously ?

(A) Use the Q output of the first FF.

(B) Use the Q output of the last FF.

(C) Tie all of the Q outputs together.

(D) Use the Q output of each FF.

48. There are .... basic types of shift register.

(A) Six

(B) Four

(C) One

(D) Many

49. A register can be used to provide data movements :

(A) Parallel Register

(B) Simple Register

(C) Shift Register

(D) All of the above

50. In this type of counter, the output of the last stage is connected to the D input of the first stage :

(A) Ring Counter

(B) Johnson Counter

(C) Straight Counter

(D) All of the above

51. ASCII code is a .... bit code.

(A) 1

(B) 2

(C) 7

(D) 8

52. Full adder can be realized using :

(A) One half adder, two OR gates

(B) Two half adder, one OR gates

(C) Two half adder, two OR gates

(D) None of the above

53. The difference bit output of a half substractor is the same as :

(A) difference bit output of a full substractor

(B) sum bit output of half adder

(C) sum bit output of full adder

(D) carry bit output of half adder

54. Which of these sets of logic gates are known as universal gates ?

(A) XOR, NAND, OR

(B) OR, NOT, XOR

(C) NOR, NAND, XNOR

(D) NOR, NAND

55. The excess-3 code for 584 is given by :

(A) 100010110111

(B) 100001110111

(C) 100010010110

(D) 100001010110

56. Why is a decoder used in digital electronics ?

(A) To convert non coded information into a binary coded form.

(B) To convert coded information into a non-coded form.

(C) It is used to divide address bus and data bus.

(D) None of the above

57. How much input and output are needed for demultiplexer ?

(A) Many outputs to one input

(B) One input many outputs

(C) One input one output

(D) None of the above

58. A .... is a table which consists of every possible combinations of inputs and its corresponding outputs.

(A) Last Table

(B) Truth Table

(C) K-Map

(D) None of the above

59. A variable on its own or in its complement form is known as :

(A) Product term

(B) Literal

(C) Sum term

(D) None of the above

60. The number of minterms for an expression comprising of 3 variables :

(A) 8

(B) 3

(C) 0

(D) 1

61. $(A + B)(A' * B') = ?$

(A) 1

(B) 0

(C) AB

(D) BA

62. The number of T flip-flop required to realise a mod-10 asynchronous counter is :

(A) 10

(B) 3

(C) 4

(D) 5

63. How many flip-flops are required to make a MOD-32 binary counter ?

   (A) 3

   (B) 45

   (C) 5

   (D) 6

64. A BCD counter is a ....

   (A) binary counter

   (B) full-modulus counter

   (C) decade counter

   (D) divide-by-10 counter

65. A shift register is a digital circuit that ....

   (A) Stores data

   (B) Shifts data from left to right

   (C) Shifts data from right to left

   (D) All of the above

66. A shift register is made of how many flip flops ?

   (A) One

   (B) Two

   (C) Three or more

   (D) None of the above

67. Which of the following shift registers can be used as both PISO and SIPO ?

   (A) 4-bit parallel-in serial-out shift register

   (B) 4-bit universal shift register

   (C) 4-bit serial-in/serial-out shift register

   (D) 4-bit parallel serial in/serial out shift

68. Which of the following is correct about serial in/serial out shift register ?

   (A) 1 input, 1 output

   (B) 1 input, 2 outputs

   (C) 2 inputs, 1 output

   (D) 2 inputs, 2 outputs

69. Which of the following digital circuits can store a bit of data and shift it left or right ?

   (A) Encoder

   (B) ADC

   (C) Multiplexer

   (D) Shift Register

70. A sequential circuit does not use clock pulses. It is :

(A) an asynchronous sequential circuit

(B) a synchronous sequential circuit

(C) a counter

(D) a shift register

71. The basic memory element in a digital circuit :

(A) consists of a NAND gate

(B) consists of a NOR gate

(C) is a flip-flop

(D) is a shift register

72. A flip-flop has two outputs which are :

(A) always 0

(B) always 1

(C) always complementary

(D) All of the above states

73. For a flip-flop with provisions of preset and clear :

(A) while presetting, clear is disabled

(B) while clearing, preset is disabled

(C) Above both are true

(D) preset and clear operations are performed simultaneously

74. The output Q_n of a J-K flip-flop is 1. It changes to 0 when a clock pulse is applied. The inputs J_n and K_n are respectively :

(A) 0 and X

(B) 1 and X

(C) X and 1

(D) X and 0

75. The characteristic equation of a D flip-flop is :

(A) $Qn + 1 = D$

(B) $Qn + 1 = Qn$

(C) $Qn + 1 = 1$

(D) $Qn + 1 = Q\bar{n}$

76. Consider the following page reference string

1 2 3 4 2 1 5 6 2 1 2 3 7 6 3 2 1 2 3 7

For optimal page replacement with 3 frames, number of page faults is :

(A) 11

(B) 12

(C) 16

(D) 14

77. Half subtractor is used to perform subtraction of ....

(A) 2 bits

(B) 3 bits

(C) 4 bits

(D) 5 bits

78. For subtracting 1 from 0, we use to take a .... from neighbouring bits.

(A) Carry

(B) Borrow

(C) Input

(D) Output

79. Let A and B is the input of a subtractor, then the output will be ....

(A) A XOR B

(B) A AND B

(C) A OR B

(D) A EXNOR B

80. The D Flip-flop has .... output/outputs.

(A) 4

(B) 1

(C) 2

(D) 3

81. The address in the main memory is known as :

(A) Logical address

(B) Physical address

(C) Memory address

(D) None of the above

82. Which of the following circuits is used to store one bit of data ?

(A) Flip-Flop

(B) Decoder

(C) Encoder

(D) Register

83. The address in the main memory is known as :

(A) Logical address

(B) Physical address

(C) Memory address

(D) None of the above

84. Which of the following memory units communicates directly with the CPU ?

(A) Auxiliary memory

(B) Main memory

(C) Secondary memory

(D) None of the above

85. In which of the following forms the computer stores its data in memory ?

(A) Hexadecimal form

(B) Octal form

(C) Binary form

(D) Decimal form

86. The invalid state for S-R latch occurs when S and R are ....

(A) both high

(B) both low

(C) S = high, R = low

(D) S = low, R = high

87. When both inputs of a J-K pulse-triggered flip-flop are LOW, and the clock triggers, what will the output be ?

(A) An invalid state will exist

(B) No change will occur in the output

(C) The output will toggle

(D) The output will reset

88. A cascaded counter, constructed by cascading a MOD 3 and a MOD 4 counters, will have :

(A) 7 states

(B) 1 state

(C) 12 states

(D) 2 states

89. The last state of a modulus-11 binary counter is ....

(A) 1011

(B) 1010

(C) 1001

(D) 1100

90. If a 10-bit Ring counter has an initial state 11 0100 0000, what is the state after the second clock pulse ?

(A) 11 0100 0000

(B) 00 1101 0000

(C) 11 0000 0000

(D) 00 0000 0000

91. A priority encoder means that :

(A) the lowest priority goes first

(B) the highest input has priority

(C) priority is programmed into the device

(D) the lowest input has priority

92. How many different states does a 3-bit asynchronous counter have ?

(A) 2

(B) 4

(C) 8

(D) 16

93. Which operation is shown in the following operation :

    $(X + Y)(X + Z)(Z + Y)$

(A) NOR

(B) ExOR

(C) SOP

(D) POS

94. Term combinations are made by placing .... cells next to each other.

(A) Adjacent

(B) Complementary

(C) Supplementary

(D) Nodes

95. What a virtual-memory miss is called ?

(A) Hit miss

(B) Page hit

(C) Page miss

(D) Page fault

96. A .... process is copied into the main memory from the secondary memory.

(A) Swapping

(B) Paging

(C) Segmentation

(D) Demand Paging

97. In FIFO page replacement algorithm, when a page is replaced what is chosen ?

(A) Oldest page is chosen

(B) Newest page is chosen

(C) Median page is chosen

(D) None of the above

98. Canonical SOP form of logic expression consists of only ....

(A) Maxterms

(B) Minterms

(C) Cells

(D) Literals

99. The addition of binary numbers $101001 + 010011$ would generate :

(A) 101110

(B) 000111

(C) 111100

(D) 010100

100. A latch is .... sensitive.

(A) Both level and edge

(B) Edge

(C) Level

(D) None of the above

4. Four alternative answers are mentioned for each question as—A, B, C & D in the booklet. The candidate has to choose the correct answer and mark the same in the OMR Answer-Sheet as per the direction :

Example :

Question :

Q. 1 (A) ● (C) (D)
Q. 2 (A) (B) ● (D)
Q. 3 (A) ● (C) (D)

Illegible answers with cutting and over-writing or half filled circle will be cancelled.

5. Each question carries equal marks. Marks will be awarded according to the number of correct answers you have.

6. All answers are to be given on OMR Answer sheet only. Answers given anywhere other than the place specified in the answer sheet will not be considered valid.

7. Before writing anything on the OMR Answer Sheet, all the instructions given in it should be read carefully.

8. After the completion of the examination candidates should leave the examination hall only after providing their OMR Answer Sheet to the invigilator. Candidate can carry their Question Booklet.

9. There will be no negative marking.

10. Rough work, if any, should be done on the blank pages provided for the purpose in the booklet.

11. To bring and use of log-book, calculator, pager and cellular phone in examination hall is prohibited.

12. In case of any difference found in English and Hindi version of the question, the English version of the question will be held authentic.

Impt. : On opening the question booklet, first check that all the pages of the question booklet are printed properly. If there is ny discrepancy in the question Booklet, then after showing it to the invigilator, get another question Booklet of the same series.

4. प्रश्न-पुस्तिका में प्रत्येक प्रश्न के चार सम्भावित उत्तर— A, B, C एवं D हैं। परीक्षार्थी को उन चारों विकल्पों में से सही उत्तर छाँटना है। उत्तर को OMR आन्सर-शीट में सम्बन्धित प्रश्न संख्या में निम्न प्रकार भरना है :

उदाहरण :

प्रश्न :

प्रश्न 1 (A) ● (C) (D)
प्रश्न 2 (A) (B) ● (D)
प्रश्न 3 (A) ● (C) (D)

अपठनीय उत्तर या ऐसे उत्तर जिन्हें काटा या बदला गया है, या गोले में आधा भरकर दिया गया, उन्हें निरस्त कर दिया जाएगा।

5. प्रत्येक प्रश्न के अंक समान हैं। आपके जितने उत्तर सही होंगे, उन्हीं के अनुसार अंक प्रदान किये जायेंगे।

6. सभी उत्तर केवल ओ. एम. आर. उत्तर-पत्रक (OMR Answer Sheet) पर ही दिये जाने हैं। उत्तर-पत्रक में निर्धारित स्थान के अलावा अन्यत्र कहीं पर दिया गया उत्तर मान्य नहीं होगा।

7. ओ. एम. आर. उत्तर-पत्रक (OMR Answer Sheet) पर कुछ भी लिखने से पूर्व उसमें दिये गये सभी अनुदेशों को सावधानीपूर्वक पढ़ लिया जाये।

8. परीक्षा समाप्ति के उपरान्त परीक्षार्थी कक्ष निरीक्षक को अपनी OMR Answer Sheet उपलब्ध कराने के बाद ही परीक्षा कक्ष से प्रस्थान करें। परीक्षार्थी अपने साथ प्रश्न-पुस्तिका ले जा सकते हैं।

9. निगेटिव मार्किंग नहीं है।

10. कोई भी रफ कार्य, प्रश्न-पुस्तिका के अन्त में, रफ-कार्य के लिए दिए खाली पेज पर ही किया जाना चाहिए।

11. परीक्षा-कक्ष में लॉग-बुक, कैलकुलेटर, पेजर तथा सेल्युलर फोन ले जाना तथा उसका उपयोग करना वर्जित है।

12. प्रश्न के हिन्दी एवं अंग्रेजी रूपान्तरण में भिन्नता होने की दशा में प्रश्न का अंग्रेजी रूपान्तरण ही मान्य होगा।

महत्वपूर्ण : प्रश्नपुस्तिका खोलने पर प्रथमतः जाँच कर देख लें कि प्रश्न-पुस्तिका के सभी पृष्ठ भलीभाँति छपे हुए हैं। यदि प्रश्नपुस्तिका में कोई कमी हो, तो कक्षनिरीक्षक को दिखाकर उसी सिरीज की दूसरी प्रश्न-पुस्तिका प्राप्त कर लें।